CP6001

R1 and R2 Versions

6U CompactPCI Processor Board based on the Intel® Core™ Duo Processor and the Intel® Core™2 Duo Processor with the Intel® 945GM Express Chipset

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User Guide

kontron

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Disclaimer

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This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.

Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.

Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.

Note ...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

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Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks.

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Special Handling and Unpacking Instructions

ESD Sensitive Device!

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Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

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General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Kontron grants the original purchaser of Kontron's products a ***TWO YEAR LIMITED HARDWARE WARRANTY*** as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of Kontron are valid unless the consumer has the express written consent of Kontron.

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If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

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Chapter 1

Introduction

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1. Introduction

1.1 Board Overview

The CP6001 is a highly integrated 6U CompactPCI CPU board based on the Intel® Core™ Duo and the Intel® Core™2 Duo microprocessors combined with the high-performance Mobile Intel® 945GM Express Chipset.

The board is capable of supporting the Intel® Core™ Duo and the Intel® Core™2 Duo processor versions in 65 nm technology with 64 kB L1 and up to 4 MB L2 cache in a 479 µFCBGA package with frequencies of 1.2 GHz and 1.5 GHz providing 533 MHz or 667 MHz front side bus speed. The CP6001 utilizes the Mobile Intel® 945GM Express Chipset as Graphics Memory Controller Hub and the ICH7R as I/O Controller Hub.

The board includes up to 4 GB of soldered, dual-channel Double Data Rate 2 (DDR2) memory. The DDR2 memory operates at 533/667 MHz, depending on the CPU. A soldered CompactFlash solution is implemented via an IDE Flash controller combined with a NAND Flash memory. The CP6001 further provides support for one optional USB 2.0 NAND Flash module.

The CP6001 offers a complete set of data, communication and multimedia interfaces, such as three Gigabit Ethernet ports (Intel® 82573L) on the front panel, two of which are switchable to rear I/O (in accordance with the PICMG CompactPCI Packet Switching Backplane Specification 2.16), one Parallel ATA interface connected to the soldered CompactFlash, two onboard Serial ATA interfaces switchable to rear I/O and two additional Serial ATA interfaces only on rear I/O, one high-resolution VGA interface (CRT), one DVI interface and one HDMI interface over rear I/O through dedicated SDVO transmitters, one PMC interface with 32-bit/66 MHz, and rear I/O with several interfaces. In addition, seven USB 2.0 ports are available on the board, two on the front panel, one onboard port for the USB 2.0 NAND Flash module, and four on rear I/O. Further interfaces include two COM ports, one RS-232 port implemented as RJ-45 connector on the front panel and routed to rear I/O, and one RS-422 port on the rear I/O. The board supports a configurable 32-bit/66 MHz, hot swap CompactPCI interface.

The CP6001 provides safety and security via a Trusted Platform Module (TPM) 1.2, two redundant firmware hubs (FWH) and Intelligent Platform Management Interface (IPMI) support.

The passively cooled CP6001 is available with E2 capabilities. The CP6001 R1 version is designed for standard application requirements in air-cooled environments and can accommodate a PMC module or an onboard 2.5" SATA HDD. The CP6001 R2 version is ruggedized for high shock and vibration environments and provides support for a conduction cooled PCI mezzanine card (CCPMC).

Designed for stability and packaged in a rugged format, the board fits into all applications situated in industrial environments, including I/O intensive applications where only one slot is available for the CPU, making it a perfect core technology for long-life applications. Components with high temperature tolerance have been selected from embedded technology programs, and therefore offer long-term availability.

The board is offered with Microsoft® Windows® XP, Windows® XP Embedded, Linux, and VxWorks operating systems. Please contact Kontron for further information concerning the operation of the CP6001 with other operating systems.

1.2 Board-Specific Information

The CP6001 is a CompactPCI single-board computer based on the Intel® Core™ Duo and the Intel® Core™2 Duo processors and specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

Some of the CP6001's outstanding features are:

- Designed to support for the following processors:
  - Intel® Core™ Duo, U2500 (ULV), 1.2 GHz, 533 MHz FSB, 2 MB L2 cache
  - Intel® Core™2 Duo, L7400 (LV), 1.5 GHz, 667 MHz FSB, 4 MB L2 cache
- 479-pin µFCBGA package
- 64 kB L1 and up to 4 MB L2 cache on-die, running at CPU speed
- Intel® 945GM and Intel® 82801GR (ICH7R) chipset
- Up to 4 GB DDR2-SDRAM memory running at 533/667 MHz
- Integrated 3D high-performance VGA controller
- Analog display support for up to 2048 x 1536 pixels at 75 Hz
- Two independent digital display interfaces: DVI and HDMI/DVI, both routed to rear I/O
- Support for up to two High Definition Audio codecs on rear I/O
- 32-bit / 66 MHz CompactPCI interface in accordance with the PICMG 2.0, Rev 3.0 spec.
- PMC interface with rear I/O support and bezel cutout on front panel and PCI functionality, 32-bit/66 MHz PCI
- Three Gigabit Ethernet interfaces utilizing an x1 lane PCI Express per GbE controller
  - Two Gigabit Ethernet interfaces on the front panel switchable to rear I/O (PICMG 2.16)
  - One Gigabit Ethernet interface on the front panel
- EIDE Ultra ATA interface for soldered CompactFlash
- Four Serial ATA interfaces
  - Two onboard Serial ATA interfaces switchable to rear I/O
  - Two Serial ATA interfaces on rear I/O
- Optional mounting kit for Serial ATA 2.5" hard disk
- Up to seven USB 2.0 ports:
  - Two ports on the front panel
  - One onboard port for the USB 2.0 NAND Flash module
  - Four ports on rear I/O
- Two COM ports (RS-232 and RS-422):
  - One RS-232 port either on the front panel or on the rear I/O
  - One RS-422 port on the rear I/O
- I/O extension connector (LPC)
- 4HP, 6U CompactPCI
- AMI BIOS
- Two 1 MB onboard FWHs for redundant BIOS
- Watchdog Timer
- Real-time clock
- Jumperless board configuration
- Passive heat sink solution for forced convection cooling
- Hot swap capability: as system controller or as peripheral device
- Supports PICMG Packet Switching Backplane Specification 2.16
- Several rear I/O configurations
- Rear I/O on J3 and J5; optionally on J4
- IPMI compliant Baseboard Management Controller

1.3 System Expansion Capabilities

1.3.1 PMC/CCPMC Module

The CP6001 has one PCI-X, 32-bit/66 MHz, rear I/O capable, PMC mezzanine interface. This interface supports a wide range of available PMC/CCPMC modules with PCI interface including all of Kontron's PMC modules and provides an easy and flexible way to configure the CP6001 for various application requirements.

The CP6001 R1 version provides support for a PMC module. The CP6001 R2 version provides support for a conduction cooled PMC (CCPMC) module.

For further information concerning the PMC interface, refer to Chapter 2.3.8, PMC Interface.

1.3.2 CP6001-MK2.5SATA Assembly Kit

The CP6001 R1 version comes with an optional CP6001-MK2.5SATA assembly kit comprised of one CP6001-EXT-SATA module and the necessary components needed for mounting the module on the board. The CP6001-EXT-SATA module is required for connecting an onboard 2.5" Serial ATA HDD or SSD to the CP6001 and can be used only on the R1 version.

For further information concerning the CP6001-EXT-SATA module, refer to Appendix A.

1.3.3 CP-RIO6-001 Rear I/O Module

The CP-RIO6-001 rear I/O module has been designed for use with the CP6001 board from Kontron and provides comprehensive rear I/O functionality.

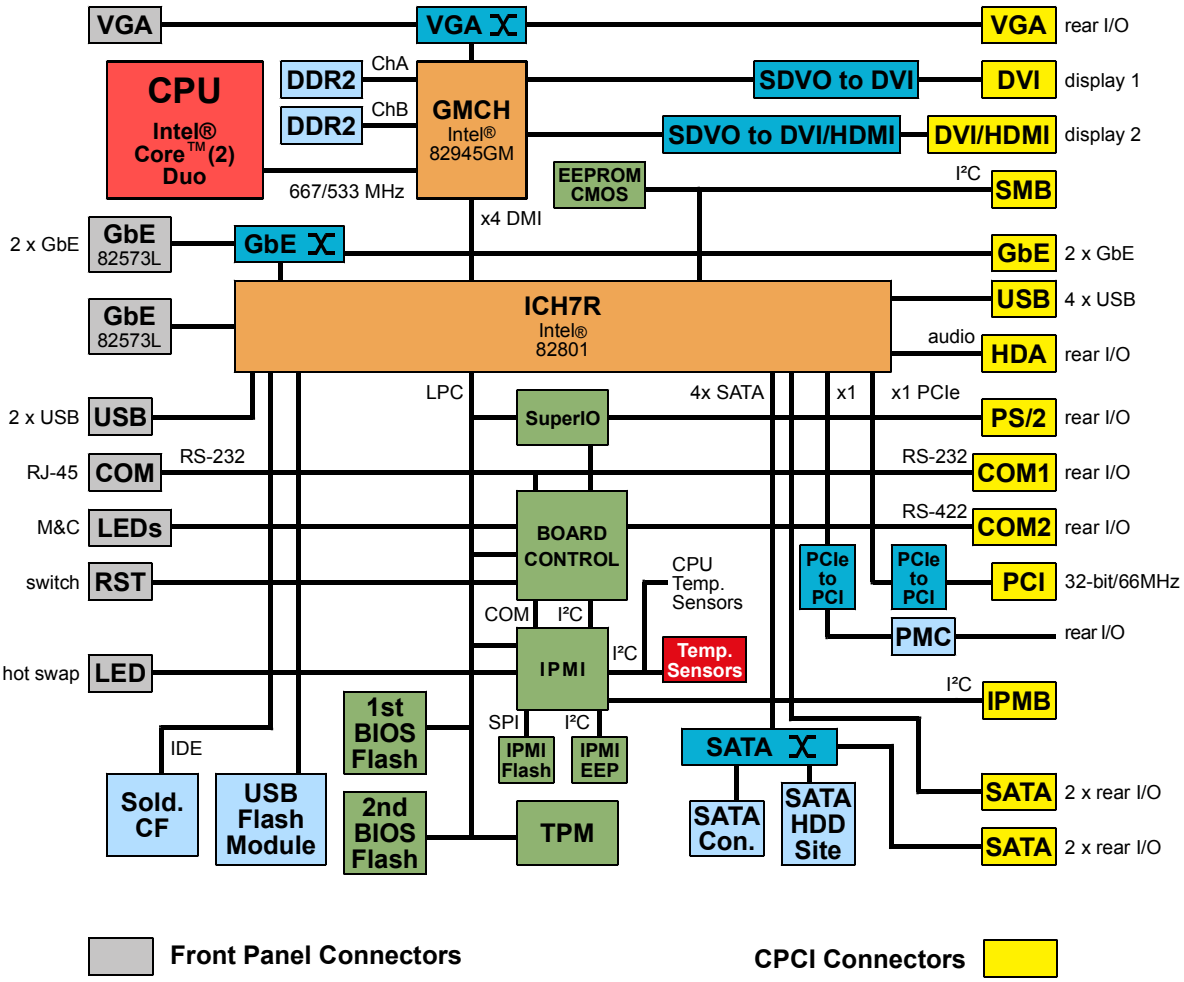
For further information concerning the CP-RIO6-001 module, refer to Appendix B.

1.4 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

1.4.1 Functional Block Diagram

Figure 1-1: CP6001 Functional Block Diagram



1.4.2 Front Panels

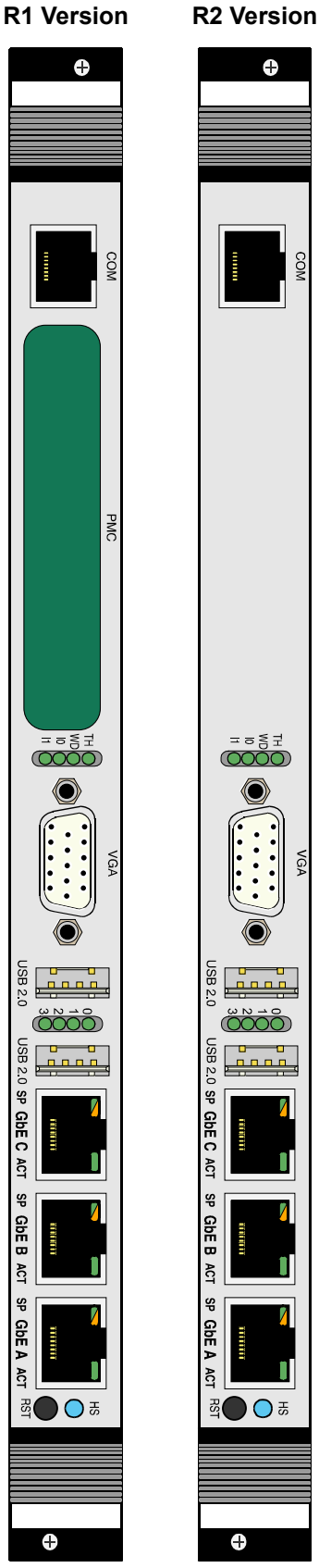


Figure 1-2: CP6001 Front Panels

Legend:

IPMI LEDs

I0/I1 (red/green): Indicate the software status of the IPMI controller

Status LEDs

WD (red/green): Watchdog Status

TH (red/green/amber): Overtemperature Status

HS (blue): Hot Swap Control

General Purpose LEDs

LED 0..3 (red/green/amber): General Purpose/POST code

Integral Ethernet LEDs

ACT (green): Ethernet Link/Activity

SPEED (green/orange): Ethernet Speed

SPEED ON (orange): 1000 Mbit

SPEED ON (green): 100 Mbit

SPEED OFF: 10 Mbit

Note ...

If the General Purpose LEDs are lit red during boot-up, a failure is indicated before the BIOS has started.

For further information, please contact Kontron.

1.4.3 Board Layout

Figure 1-3: CP6001 Board Layout – Front View – R1 Version

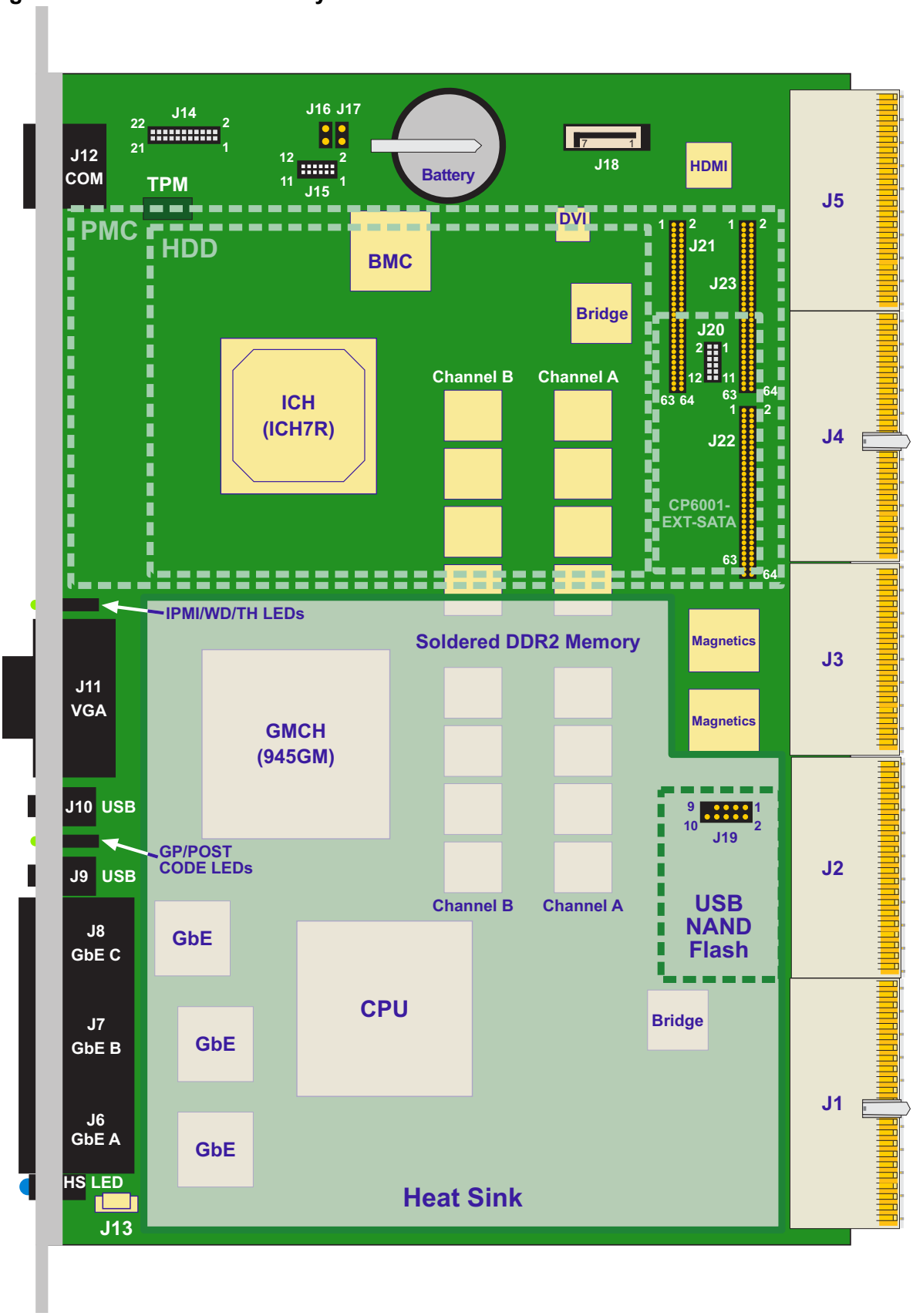


Figure 1-4: CP6001 Board Layout – Front View – R2 Version

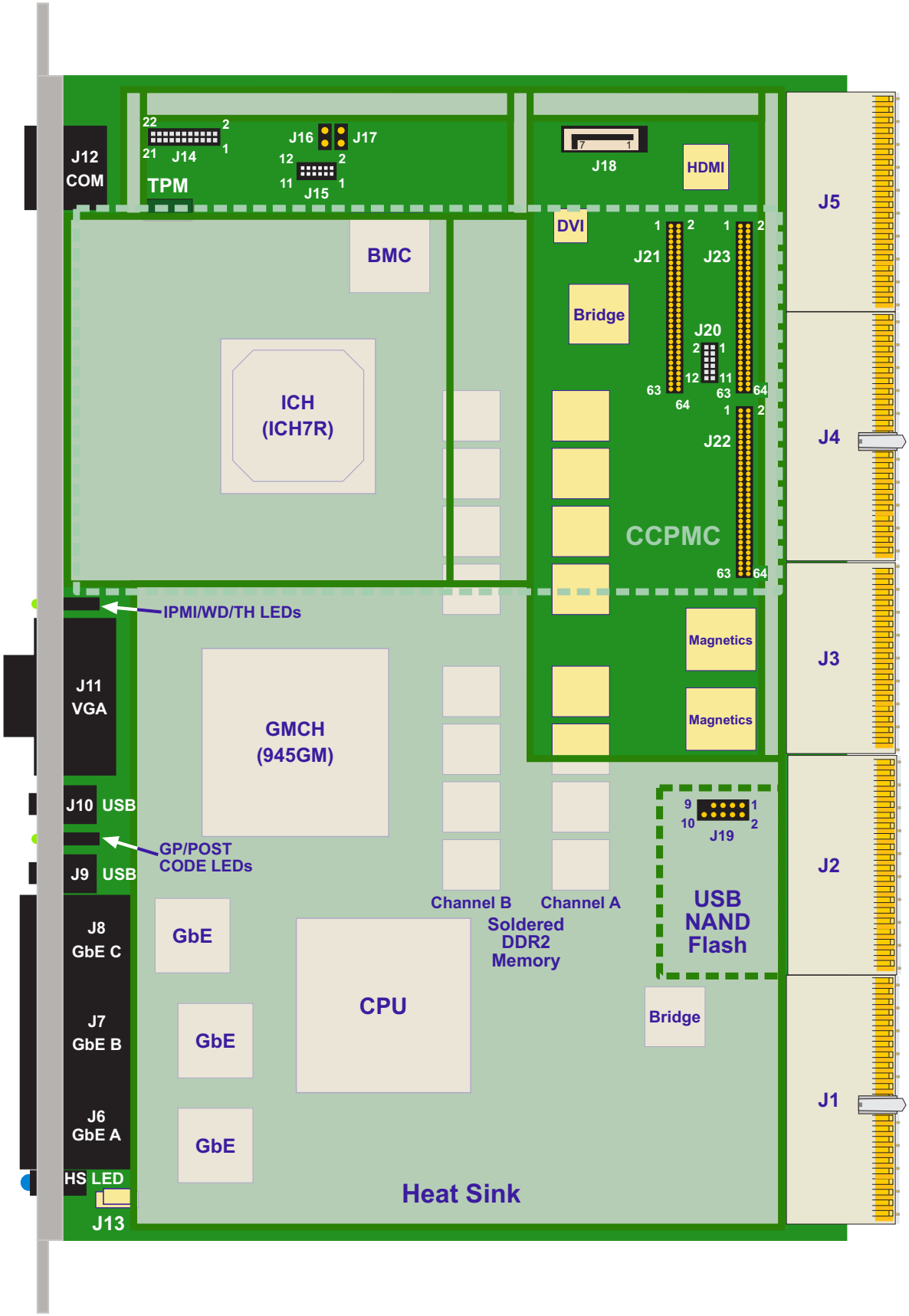
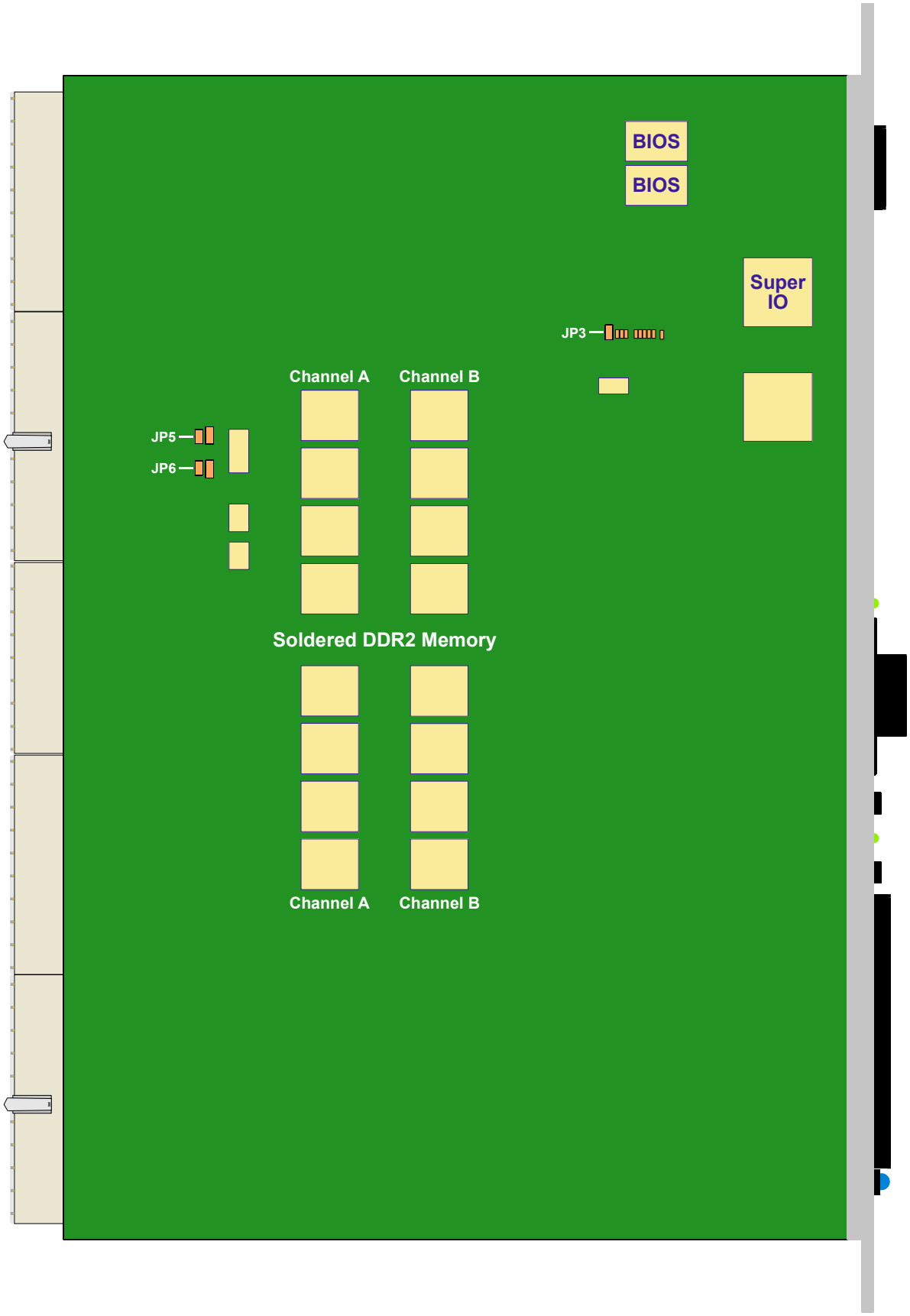


Figure 1-5: CP6001 Board Layout – Reverse View



1.5 Technical Specification

Table 1-1: CP6001 Main Specifications

CP6001		SPECIFICATIONS
Processor and Memory	CPU	The CP6001 supports the following microprocessors: • Intel® Core™ Duo, U2500 (ULV), 1.2 GHz, 533 MHz FSB, 2 MB L2 cache • Intel® Core™2 Duo, L7400 (LV), 1.5 GHz, 667 MHz FSB, 4 MB L2 cache All microprocessors are provided in a 479 µFCBGA packaging.

	Memory	Main Memory:
		• Up to 4 GB dual-channel, DDR2 memory running at 533/667 MHz
		Cache structure:
		• 64 kB L1 on-die full speed processor cache
		  • 32 kB for instruction cache
		  • 32 kB for data cache
		• Up to 4 MB L2 on-die full speed processor cache
		FLASH Memory:
		• Soldered CompactFlash (true IDE mode)
		• Two 1 MB onboard FWHs for redundant BIOS
		Memory Extension:
		• USB 2.0 NAND Flash
		Serial EEPROM:
		• 24LC64 (64 kbit)

Chipset	Intel® 945GM Express GMCH	Mobile Intel® 945GM Express Graphics Memory Controller Hub: • Support for a single Intel® Core™ Duo or Core™2 Duo microprocessor • 64-bit AGTL/AGTL+ based System Bus interface up to 667 MHz • System Memory interface with optimized support for dual-channel DDR2 SDRAM memory at 533/667 MHz without ECC • Integrated 2D and 3D Graphics Engines • Integrated 400 MHz RAMDAC

	Intel® ICH7R	Intel® 82801GR I/O Controller Hub (ICH7R):
		• Power management logic support
		• Enhanced DMA controller, interrupt controller, and timer functions
		• Integrated IDE controller Ultra ATA/100/66/33 and PIO mode
		• USB 2.0 host interface with up to seven USB ports
		• SATA Host Controller with four ports, 3 Gbit/s transfer rate
		• Five of the six x1 PCI Express ports are used on the CP6001:
		  • Three x1 PCI Express ports are used for Gigabit Ethernet
		  • Two x1 PCI Express ports are used for the PCI bridges
		• System Management Bus (SMBus) compatible with most I²C™ devices
		• Low Pin Count (LPC) interface
		• Firmware Hub (FWH) interface support

Table 1-1: CP6001 Main Specifications (Continued)

CP6001		SPECIFICATIONS
Interfaces	CompactPCI	Compliant with CompactPCI Specification PICMG 2.0 R3.0: • System controller operation • 32-bit/66 MHz PCI/PCI-X master interface with support for up to 7 peripheral boards • 3.3V or 5V signaling levels (universal signaling support) Compliant with Packet Switching Specification PICMG 2.16 R1.0 When the CP6001 is operated in a peripheral slot, the CompactPCI bus is electrically isolated (passive mode).
	Rear I/O	The following interfaces are routed to the rear I/O connector J3, J4 and J5: • COM1 and COM2 (RS-232 and RS-422 signaling); no buffer on the rear I/O module is necessary • 4 x USB 2.0 • CRT VGA, DVI, HDMI • PS/2 (Mouse/Keyboard) • 2 x Gigabit Ethernet (compliant with PICMG 2.16, R 1.0) • 4 x SATA • PMC/CCPMC rear I/O
	Hot Swap Compatible	The board supports System Master hot swap functionality and application dependent hot swap functionality when used in a peripheral slot. When used as a System Master the board supports individual clocks for each slot and ENUM signal handling is in compliance with the PICMG 2.1 Hot Swap Specification.
	VGA	Built-in Intel 3D Graphics accelerator for enhanced graphics performance. • Supports resolutions of up to 2048 x 1536 at a 75 Hz refresh rate • Hardware motion compensation for software MPEG2 decoding • Dynamic Video Memory Technology (DVMT3.0)
	Gigabit Ethernet	Up to three 10 Base-T/100 Base-TX/1000 Base-T Gigabit Ethernet interfaces based on three Intel® 82573L Ethernet PCI Express bus controllers. • Two RJ-45 connectors on front panel switchable to rear I/O (PICMG 2.16) • One RJ-45 connector on the front panel • Automatic mode recognition (Auto-Negotiation) • Automatic cabling configuration recognition (Auto MDI-X) Cabling requirement: Category 5, UTP, four-pair cabling
	USB	Seven USB 2.0 ports supporting UHCI and EHCI: • Two type A connectors on the front panel • Four ports on the rear I/O interface • One onboard connector for the USB 2.0 NAND Flash module

Table 1-1: CP6001 Main Specifications (Continued)

CP6001		SPECIFICATIONS
Interfaces	Serial	Two 16C550-compatible UARTs on the rear I/O interface, one for RS-232 and one for RS-422 signaling. The UART for RS-232 signaling is also routed to the front panel.
	PMC / CCPMC	CMC/PMC P1386/Draft 2.4a and CCPMC VITA 20-2001 (R2005) compliant mezzanine interface: • PMC module support only on the R1 version if no HDD is installed • CCPMC module support on the R2 version • Jn1, Jn2 and Jn4 PCI mezzanine connectors for standard PMC modules • 32-bit/66 MHz PCI/PCI-X interface • Rear I/O supported through the CompactPCI connector J4 • Supported voltages: 3.3 V, 5 V, +12 V, and -12 V • Supports 3.3 V signaling voltage (VI/O)
	Keyboard and Mouse	Keyboard and mouse are supported • USB Support • PS/2 (keyboard and mouse) on rear I/O

	Mass Storage	EIDE ATA:
		• One onboard ATA interface for the soldered CompactFlash
		SATA: Integrated Serial ATA Host Controllers
		• Provide independent DMA operation on 4 channels:
		  • Two onboard SATA interfaces switchable to rear I/O via BIOS
		  • Two SATA interfaces only on rear I/O
		• Data transfer rates up to 300 MBs
		Onboard 2.5" hard disk:
		• Onboard 2.5" hard disk is supported via a 22-pin Serial ATA interface on the CP6001-EXT-SATA module

	I/O Extension Interface	I/O extension interface: • LPC devices
Sockets	Front Panel Connectors	• VGA: 15-pin, D-Sub connector • USB: two type A connectors • Ethernet: three RJ-45 connectors • COM: 8-pin, RJ-45 connector • PMC front panel (only on R1)

	Onboard Connectors	• USB 2.0 NAND Flash connector, J19
		• I/O extension connector, J14
		• PMC connectors J21 - J23 (Jn1, Jn2 and Jn4)
		• Two SATA connectors:
		  • One 7-pin, standard SATA connector with locking mechanism, J18
		  • One 12-pin, SATA extension connector, J20
		• CompactPCI Connector J1 to J3 (J4 - J5 optional)
		• J15 for factory use only

Table 1-1: CP6001 Main Specifications (Continued)

CP6001		SPECIFICATIONS
HW Monitoring	LEDs	System Status LEDs: • I0/I1 (red/green): Indicate the software status of the IPMI controller • WD (red/green): Watchdog Status • TH (red/green/amber): Overtemperature Status • HS (blue): Hot Swap Control General Purpose LEDs: • LED 0..3 (red/green/amber): General Purpose / POST code Gigabit Ethernet Status: • ACT (green): Ethernet Link/Activity • SPEED (green / orange): Ethernet Speed • SPEED ON (orange): 1000 Mbit • SPEED ON (green): 100 Mbit • SPEED OFF: 10 Mbit
	Watchdog	Software configurable Watchdog generates IRQ or hardware reset.

	Thermal-Related Functions	Thermal monitor and control:
		• Onboard temperature sensors:
		  • Temp1 sensor
		  • Temp2 sensor
		  • Temperature sensor integrated in the Super I/O
		• Processor thermal monitoring and regulation:
		  • Intel® Thermal Monitor (TM1 and TM2)
		  • Intel® SpeedStep®
		  • Catastrophic cooling failure sensor
		  • Two Digital Thermal Sensors (one per core)
		  • Thermal Diode Sensor
		• Convection cooling

	System Monitor	In SCH3112 integrated hardware monitor for supervision of: • Two fan speed inputs • Board temperature
	IPMI	Baseboard Management Controller (BMC) that supports two keyboard controller-style interfaces (KCS) compliant with: • IPMI specification v1.5 • PICMG 2.9 specification IPMI supports two IPMB busses via the J1 and J2 connectors.

Table 1-1: CP6001 Main Specifications (Continued)

CP6001		SPECIFICATIONS

Software	Software BIOS	AMI BIOS with 1 MB Flash memory with the following features:
		• User BIOS defaults (Setup Default Override - SDO)
		• ACPI support
		• FWH write protection (BIOS Flash)
		• Manufacturing data:
		  • Serial number
		  • Material number
		  • Chipset revision
		  • CPU microcode
		• QuickBoot
		• QuietBoot
		• LAN boot capability for diskless systems (standard PXE)
		• Boot from USB floppy disk drive
		• USB keyboard emulation during BIOS boot
		• Plug and Play capability
		• BIOS parameters are saved in the EEPROM
		• Hardware Health Monitoring

	Operating Systems	Operating systems supported: • Microsoft® Windows® XP • Microsoft® Windows® XP Embedded • Linux • VxWorks Please contact Kontron for further information concerning the operation of the CP6001 with other operating systems.

Table 1-1: CP6001 Main Specifications (Continued)

	CP6001	SPECIFICATIONS
General	Mechanical	6U, 4HP, CompactPCI compliant form factor
	Power Consumption	See Chapter 5 for details
	Temperature Ranges	Operational: 0°C to +60°C Standard -40°C to +85°C E2, optional (TPM: -25°C to +70°C) Storage: -55°C to +85°C Without battery or any additional components  ***Note ...*** When a battery is installed, refer to the operational specifications of the battery as this determines the board's storage temperature (See "Battery" below).  ***Note ...*** When additional components are installed, refer to their operational specifications as this will influence the board's operational and storage temperature.
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	233.35 mm x 160 mm
	Board Weight	R1: 630 g (4HP with front panel and heat sink and without mezzanine boards) R2: 650 g (4HP with front panel, heat sink and stiffeners and without mezzanine boards)
	Battery	The CP6001 R1 version provides a 3.0V lithium battery for RTC with battery socket. Recommended type: CR2025 Temperature ranges: Operational: -20°C to +70°C typical (refer to the battery manufacturer's specifications for exact range) Storage: -55°C to +70°C typical (no discharge)

1.6 Kontron Software Support

Kontron is one of the few CompactPCI and VME manufacturers providing inhouse support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software manufacturers, *Kontron* is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

1.7 Standards

The board complies with the requirements of the following standards:

Table 1-2: Standards for the CP6001 R1 and R2 versions

TYPE	ASPECT	STANDARD	REMARKS
CE	Emission	EN55022 EN61000-6-3	--
	Immission	EN55024 EN61000-6-2	--
	Electrical Safety	EN60950-1	--
Mechanical	Mechanical Dimensions	IEEE 1101.10	--
Environmental	Climatic Humidity	IEC60068-2-78	--
	Generic Environmental	ANSI/VITA 47	--
	WEEE	Directive 2002/96/EC	Waste electrical and electronic equipment
	RoHS	Directive 2002/95/EC	Restriction of the use of certain hazardous substances in electrical and electronic equipment
	Vibration (Sinusoidal)	IEC61131-2 IEC60068-2-6	Test parameters: • 5-150 (Hz) frequency range • 1 (g) acceleration • 1 (oct/min) sweep rate • 10 cycles/axis • 3 axes
	Single Shock	IEC61131-2 IEC60068-2-27	Test parameters: • 15 (g) acceleration • 11 (ms) pulse duration • 3 shocks per direction • 6 directions • 5 (s) recovery time

The test parameters indicated in the table below are valid only if the CP6001 R2 version is operated in a chassis with the capability to fixate the board's upper and lower card edges. The front panel I/O performance may be reduced if the board is operated in accordance with the ANSI/VITA 47 Class V2 specification. For full performance in accordance with the ANSI/VITA 47 Class V2 specification, use the CompactPCI and rear I/O ports.

Table 1-3: Additional Standards for the CP6001 R2 Version

TYPE	ASPECT	STANDARD	REMARKS
Environmental	Random Vibration (Broadband)	ANSI/VITA 47 Class V2 MIL-STD-810E Method 514 Procedure I	Test parameters: • 5-100 (Hz) frequency range; +3 (dB) slope • 100-1000 (Hz) frequency range; 0.04 (g^2/Hz) PSD • 1000-2000 (Hz) frequency range; -6 (dB) slope • 60 (min) test duration / axis • 3 axes
	Single Shock	ANSI/VITA 47 Class V2 MIL-STD-810E Method 516 Procedure I	Test parameters: • 20 (g) acceleration • 11 (ms) pulse duration (half-sine) • 3 shocks per direction • 6 directions • 5 (s) recovery time

1.8 Related Publications

The following publications contain information relating to this product.

Table 1-4: Related Publications

PRODUCT	PUBLICATION
CompactPCI Systems and Boards	CompactPCI Specification 2.0, Rev. 3.0 CompactPCI Packet Switching Backplane Specification PICMG 2.16 Rev. 1.0 CompactPCI System Management Specification PICMG 2.9 Rev. 1.0 CompactPCI Hot Swap Specification PICMG 2.1 Rev. 2.0
	IPMI - Intelligent Platform Management Interface Specification v1.5
	Kontron CompactPCI Backplane Manual, ID 24229
CompactFlash Cards	CF+ and CompactFlash Specification Revision 2.1
PMC Module	IEEE 1386-2001, IEEE Standard for a Common Mezzanine Card (CMC) Family IEEE 1386.1-2001, IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)
CCPMC Modules	VITA 20-2001 (R2005)
All Kontron products	Product Safety and Implementation Guide, ID 1021-9142

Chapter 2

Functional Description

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2. Functional Description

2.1 CPU, Memory and Chipset

2.1.1 CPU

The CP6001 supports the latest Intel® Core™ Duo and Intel® Core™2 Duo processor family up to speeds of 1.5 GHz with up to 667 MHz FSB.

The Intel® Core™ Duo consists of two cores and up to 2 MB L2 cache shared by both cores. The Intel® Core™2 Duo consists of two cores, up to 4 MB L2 cache shared by both cores, Intel® Extended Memory 64 Technology (Intel® EM64T), and enhanced address range for up to 64 GB memory. The Intel® Core™ Duo and the Intel® Core™2 Duo processors deliver optimized power-efficient computing and outstanding dual-core performance with low power consumption.

The Intel® Core™ Duo and the Intel® Core™2 Duo support Intel's latest Virtualization Technology (VT), which allows a platform to run multiple operating systems and applications in independent partitions, such as performing system upgrades and maintenance without interrupting the system or the application, keeping software loads and virus attacks separate, combining multiple servers in one system, etc. With processor and I/O enhancements to Intel's various platforms, Intel Virtualization Technology improves the performance and robustness of today's software-only virtual machine solutions.

Furthermore, the Intel® Core™ Duo and the Intel® Core™2 Duo also support the Intel® SpeedStep® technology which enables real-time dynamic switching of the voltage and frequency between several modes. This is achieved by switching the bus ratios, core operating voltage, and core processor speeds without resetting the system. The frequency for the processor may also be selected in the BIOS or via the operating system.

The following list sets out some of the key features of the Intel® Core™ Duo and the Intel® Core™2 Duo processors:

- Two mobile execution cores in one single processor
- Support of Intel's Virtualization Technology (Vanderpool)
- Support of Intel Architecture with Dynamic Execution
- Outstanding dual-core performance with low power consumption
- On-die, primary 32 kB instruction cache and 32 kB write-back data cache
- On-die, L1 and L2 cache with Advanced Transfer Cache Architecture
- Advanced Branch Prediction and Data Prefetch Logic
- Streaming SIMD Extensions 3 (SSE3)
- Up to 667 MHz, Source-Synchronous Front Side Bus (FSB)
- Advanced Power Management features including Enhanced Intel® SpeedStep® technology
- Intel® Extended Memory 64 Technology for 64-bit computing (only with the Intel® Core™2 Duo)

The following tables indicate the Intel® Core™ Duo and the Intel® Core™2 Duo processors supported on the CP6001, their maximum power dissipation and their frequency in the various SpeedStep® modes.

Table 2-1: Processors Supported on the CP6001

SPEED	Core™ Duo 1.2 GHz (ULV[1]) 2 MB L2 Cache	Core™2 Duo 1.5 GHz (LV[2]) 4 MB L2 Cache
PACKAGE	µFCBGA	µFCBGA
L2 CACHE	2 MB	4 MB
FSB	533 MHz	667 MHz

[1]ULV: Ultra Low Voltage
[2]LV: Low Voltage

Table 2-2: Maximum Power Dissipation of the Processors (CPU only)

FREQUENCY MODE	Core™ Duo 1.2 GHz (ULV) 2 MB L2 Cache	Core™2 Duo 1.5 GHz (LV) 4 MB L2 Cache
Maximum Power HFM[3]	9.0 W	17 W
Maximum Power LFM[4]	7.5 W	15 W

[3]HFM High Frequency Mode (maximum frequency of the CPU)
[4]LFM Low Frequency Mode (frequency is 1.0 GHz for 667 MHz FSB and 800 MHz for 533 MHz FSB)

Table 2-3: CPU Frequency in the Various SpeedStep® Modes

FREQUENCY	Core™ Duo 1.2 GHz (ULV) 2MB L2 Cache	Core™2 Duo 1.5 GHz (LV) 4 MB L2 Cache
2.16 GHz	--	--
2.0 GHz	--	--
1.66 GHz	--	--
1.5 GHz	--	x
1.33 GHz	--	--
1.2 GHz	x	--
1.0 GHz	--	x
800 MHz	x	--

2.1.2 Memory

The CP6001 supports a dual-channel DDR2 memory without Error Checking and Correcting (ECC) running at 533/667 MHz (PC2-4200 or PC2-5300). The maximum memory size per channel is 2 GB. The available memory configuration can be either 2 GB or 4 GB. However, due to internal memory allocations, the amount of memory available to applications is less than the total physical memory in the system. For example, the chipset's Dynamic Video Memory Technology (DVMT 3.0) dynamically allocates the proper amount of system memory required by the operating system and the application.

Table 2-4: Supported Memory Configurations

CHANNEL A (Soldered)	CHANNEL B (Soldered)	TOTAL PHYSICAL MEMORY	TOTAL MEMORY AVAILABLE TO APPLICATIONS
1 GB	1 GB	2 GB	2 GB minus the allocated memory for DVMT
2 GB	2 GB	4 GB	3.5 GB minus the allocated memory for DVMT and cPCI/PMC/CCPMC devices

2.1.3 Intel® 945GM Express Chipset Overview

The Intel® 945GM Express Chipset consists of the following devices:

- Mobile Intel® 945GM Express Chipset Graphics Memory Controller Hub (945GM Express Chipset GMCH)
- I/O Controller Hub 7 (ICH7R)

The 945GM Express Chipset GMCH provides the processor interface for the Intel® Core™ Duo and the Intel® Core™2 Duo microprocessors and two DDR2 channels, and includes a high-performance graphics accelerator. The ICH7R is a centralized controller for the boards' I/O peripherals, such as the PCI, PCI Express, USB 2.0, SATA II, IDE and LPC ports.

2.1.4 Mobile Intel® 945GM Express Chipset GMCH

The Mobile Intel® 945GM Express Chipset Graphics Memory Controller Hub (945GM Express Chipset GMCH) is a highly integrated hub that provides the CPU interface (optimized for the Intel® Core™ Duo and the Intel® Core™2 Duo microprocessors), two DDR2 SDRAM system memory interfaces at 533MHz or 667MHz, a hub link interface to the ICH7R and high-performance internal graphics.

Graphics and Memory Controller Hub Feature Set

Host Interface

The 945GM Express Chipset GMCH is optimized for the Intel® Core™ Duo and the Intel® Core™2 Duo microprocessors. The chipset supports Front Side Bus (FSB) frequencies of 533 MHz or 667 MHz using 1.05 V AGTL signaling. The AGTL bus supports 32-bit host addressing for decoding up to 4 GB memory address space.

System Memory Interface

The 945GM Express Chipset GMCH integrates a dual-channel DDR2 SDRAM controller with two 64-bit wide interfaces without ECC bits. The chipset supports DDR533 and DDR667 DDR2 SDRAM for system memory.

945GM Express Chipset GMCH

The 945GM Express Chipset GMCH includes a highly integrated graphics accelerator delivering high-performance 3D and 2D graphic capabilities. The internal graphics controller provides an interface for a standard analog VGA display and two SDVO interfaces for TMDS® devices.

2.1.5 I/O Controller Hub (ICH7R)

The ICH7R is a highly integrated multifunctional I/O Controller Hub that provides the interface to the PCI Bus and integrates many of the functions needed in today's PC platforms, for example, PCI Express, Ultra DMA 100/66/33 IDE controller, SATA controller, USB host controller supporting USB 2.0, LPC interface, and a FWH Flash BIOS interface controller. The ICH7R communicates with the host controller over a dedicated hub interface.

I/O Controller Hub feature set comprises:

- Bus master IDE controller UltraDMA 100/66/33 or PIO mode
- Five USB controllers with up to eight USB 1.1 or USB 2.0 ports (max. of 7 ports available)
- Hub interface for a 945GM Express Chipset
- FWH interface
- LPC interface
- RTC controller

2.2 Peripherals

The following standard peripherals are available on the CP6001 board:

2.2.1 Timer

The CP6001 is equipped with the following timers:

- Real-time clock
  The ICH7R contains a MC146818A compatible real-time clock with 256 bytes of battery-backed RAM.
  The real-time clock performs timekeeping functions and includes 256 bytes of general purpose battery-backed CMOS RAM. All CMOS RAM data from the RTC remains stored in an additional EEPROM. Further features include an alarm function, programmable periodic interrupt and a 100-year calendar.
  The R1 version provides a battery, which is used for the timekeeping function. On the R2 version, the RTC will be reset after the board is powered off.
- Hardware delay timer for short reliable delay times

2.2.2 Watchdog Timer

A user-configurable Watchdog Timer with four different modes of operation is available. For further information on the Watchdog Timer, refer to Chapter 4.4.12, Watchdog Timer Control Register.

2.2.3 Battery

The R1 version is provided with a 3.0 V “coin cell” lithium battery for the RTC.

To replace the battery, proceed as follows:

- Turn off power
- Remove the battery
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. A suitable battery type is CR2025.

Note ...

The user must be aware that the battery’s operational temperature range is less than the storage temperature range of the CP6001.

For exact range information, refer to the battery manufacturer’s specifications.

Note ...

Care must be taken to ensure that the battery is correctly replaced.

The battery should be replaced only with an identical or equivalent type recommended by the manufacturer.

Dispose of used batteries according to the manufacturer’s instructions.

The typical life expectancy of a 170 mAh battery (CR2025) is 5 - 6 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and the standby time (shutdown time) of the system in which it operates.

To ensure that the lifetime of the battery has not been exceeded, it is recommended to exchange the battery after 4 - 5 years.

2.2.4 Reset

A reset will be generated under the following conditions:

- +5 V supply falls below 4.7 V (typ.)
- +3.3 V supply falls below 3.1 V (typ.)
- Power failure of at least one onboard DC/DC converter
- Push-button "RESET" pressed (on the front panel)
- Watchdog expired
- CompactPCI backplane PRST input
- CompactPCI backplane RST input (software configurable when the board is in peripheral mode)

The CP6001 responds to any of these sources by initializing local peripherals.

2.2.5 SMBus Devices

The CP6001 provides a System Management Bus (SMBus) for access to several system monitoring and configuration functions. The SMBus consists of a two-wire I²C bus interface. The following table describes the function and address of every onboard SMBus device.

Table 2-5: SMBus Device Addresses

DEVICE	SMB ADDRESS
EEPROM 24LC64	1010111xb
Clock (core)	1101001xb
Clock (PCI Express)	1101110xb
SPD (channel A)	1010000xb
SPD (channel B)	1010010xb

2.2.6 Thermal Management/System Monitoring

The SCH3112 can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds and temperatures, all of which are very important for the proper operation and stability of a high-end computer system. The SCH3112 provides an LPC interface.

The +12 V, +5 V, +3.3 V, +2.5 V, battery and Vcore voltages are supervised. Two fan tachometer outputs can be measured using the SCH3112's FAN inputs.

The temperature sensor on the SCH3112 monitors the internal temperature of the SCH3112.

2.2.7 Serial EEPROM

This EEPROM interfaces with the ICH7R via the SMBus and provides non-volatile storage for various functions including redundant CMOS RAM data and user data. In addition, a hardware write-protection function is provided, which can be configured via the rear I/O signal SYS_WP#. Fur further information, refer to Chapter 4.2, Write Protection for Non-Volatile Memory Devices.

Table 2-6: EEPROM Address Map

ADDRESS	FUNCTION
0x000 - 0x0FF	CMOS back-up
0x100 - 0x1FF	Production data
0x200 - 0x3FF	OS Boot parameter
0x400 - 0x1FFF	User

2.2.8 FLASH Memory

There are up to four Flash devices available as described below, two for the BIOS and two for data storage.

2.2.8.1 BIOS FLASH (Firmware Hub)

The CP6001 provides two redundant Firmware Hub Flash chips (2x1MB). The fail-over mechanism for the BIOS recovery can be controlled via the BMC controller or the respective jumper. If one Firmware Hub Flash is corrupted, the BMC can enable the second Firmware Hub Flash and boot the system again.

Write-protection functionality is included, which can be configured either via the BIOS or the rear I/O signal SYS_WP#. For further information, refer to Chapter 4.2, Write Protection for Non-Volatile Memory Devices.

2.2.8.2 USB 2.0 NAND Flash Module

The CP6001 supports one optional USB 2.0 NAND Flash module qualified by Kontron. The USB 2.0 NAND Flash module is connected to the onboard connector J19.

The USB 2.0 NAND Flash module is a USB 2.0 based NAND Flash drive with a built-in full hard-disk emulation and a high data transfer rate. It is optimized for embedded systems providing high-performance, reliability and security.

2.2.8.3 CompactFlash Controller

The CP6001 provides one soldered CompactFlash, i.e. NAND Flash in combination with a dedicated IDE Flash controller which is connected to the IDE port of the ICH7R. The IDE Flash controller supports the following modes: true IDE, Multiword DMA and Ultra DMA.

The IDE Flash controller provides dynamic wear leveling to spread the Flash writes across all unused memory address space. However, as the CompactFlash device has a limited number of write/erase cycles, excessive wear will occur if only a small amount of free memory space is available for use on the CompactFlash device.

Note ...

The system integrator must ensure that sufficient memory space is available to avoid damaging the CompactFlash device as a result of excessive write/erase cycles.

Write-protection functionality is included, which can be configured either via the BIOS or the rear I/O signal SYS_WP#. For further information, refer to Chapter 4.2, Write Protection for Non-Volatile Memory Devices.

2.2.9 Trusted Platform Module (TPM) 1.2

The Trusted Platform Module (TPM) 1.2 is a security chip specifically designed to provide enhanced hardware and software-based data and system security. It stores sensitive data such as encryption and signature keys, certificates and passwords, and is able to withstand software attacks to protect the stored information.

Hardware features of the TPM 1.2:

- TCG 1.2 compliant Trusted Platform Module (TPM)
- Security architecture based on Infineon SLE66CXxxPE security controller family
- EEPROM for TCG firmware enhancements and for user data and keys
- Advanced Crypto Engine (ACE) with RSA support up to 2048-bit key length
- Hardware accelerator for SHA-1 hash algorithm
- True Random Number Generator (TRNG)
- Tick counter with tamper detection
- Protection against Dictionary Attack
- Intel® Trusted Execution Technology Support
- Microsoft's recommended GPIO included
- Full personalization with Endorsement Key (EK) and EK certificate
- Power saving sleep mode

Note ...

TPM is able to operate within the temperature range of -25°C to +70°C.

Boards with E2 capabilities operated within the E2 temperature limits but outside the TPM temperature range will continue to operate without the TPM functionality.

2.3 Board Interfaces

2.3.1 Front Panel LEDs

The CP6001 is equipped with two IPMI LEDs (I0 and I1), one Watchdog LED (WD), one Overtemperature LED (TH), four General Purpose/POST code LEDs (LED0..3), and one Hot Swap LED (HS). Their functionality is described in the following chapters and reflected in the registers mentioned in Chapter 4, Configuration.

2.3.1.1 IPMI LEDs and Hot Swap LED

The IPMI LEDs I0 and I1 show the software status of the IPMI controller. The Hot Swap LED is controlled via IPMI and indicates when the shutdown process is finished and the board is ready for extraction.

The following table indicates the function of the IPMI LEDs and Hot Swap LED.

Table 2-7: IPMI LEDs and Hot Swap LED Function

IPMI LED	COLOR	NORMAL MODE	OVERRIDE MODE
I0 (right)	red	Off = module powered / running	Selectable by user
		On = module out of service	
	green	Pulsing = traffic on the IPMB-L bus	
I1 (left)	red	Any action = health error detected	Selectable by user
	green	Any action = no health error detected	
	red/green	Blinking slow = BMC running showing its heart beat Pulsing = KCS interface active	
HS LED	blue	On = ready for hot swap (board may be extracted) Off = board in normal operation (do not extract the board) Blinking = change of status to On/Off	Selectable by user: • Only lamp test

2.3.1.2 Watchdog LED and Overtemperature LED

The CP6001 provides one LED for Watchdog (WD LED) and one for Overtemperature (TH LED) status.

Note ...

If the TH LED flashes red and green at regular intervals, it indicates that the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Upon assertion of Thermtrip, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature.

Once activated, Thermtrip remains latched until a cold restart of the board is undertaken (all power off and then on again).

Table 2-8: Watchdog LED and Overtemperature LED Function

LED	COLOR	FUNCTION DURING BOOT-UP	DEFAULT FUNCTION AFTER BOOT-UP
WD LED	red/ green	The WD LED is not lit during boot-up.	Watchdog Status The WD LED states are: • Off: Watchdog inactive • Green: Watchdog active, waiting to be triggered • Red: Watchdog expired
TH LED	red/ green/ amber	The TH LED is not lit during boot-up.	Overtemperature Status The TH LED states are: • Green: If the CPU temperature is below 100°C • Amber: In case of overtemperature of the CPU, i.e. the CPU has reached a temperature above 100°C • Red/green blinks: If the CPU has been shut off, i.e. the CPU has reached a temperature above 125°C

2.3.1.3 General Purpose LEDs

The CP6001 provides four General Purpose LEDs (LED0..3) designed to indicate the boot-up POST code and available to the application as General Purpose LEDs.

If the LED0..3 are lit red during boot-up, a failure is indicated before the BIOS has started. In this case, check the power supply. If the power supply appears to be functional and the LEDs are still red, please contact Kontron for further assistance.

The POST code is indicated during the boot-up phase. After boot-up, the LEDs indicate General Purpose or Port 80 signals, depending on the BIOS settings. The default setting after boot-up is General Purpose.

Table 2-9: General Purpose LED Function

LED	COLOR	FUNCTION DURING BOOT-UP	FUNCTION DURING BIOS POST (if POST code config. is enabled)	DEFAULT FUNCTION AFTER BOOT-UP
LED3	red	When lit up during boot-up, it indicates a BIOS boot failure	--	General Purpose or Port 80, freely configurable*
	green	--	BIOS POST bit 3 and bit 7	
	amber	--	--	
LED2	red	When lit up during boot-up, it indicates a BIOS boot failure	--	General Purpose or Port 80, freely configurable*
	green	--	BIOS POST bit 2 and bit 6	
	amber	--	--	
LED1	red	When lit up during boot-up, it indicates a hardware reset.	--	General Purpose or Port 80, freely configurable*
	green	--	BIOS POST bit 1 and bit 5	
	amber	--	--	
LED0	red	When lit up during boot-up, it indicates a power-on reset.	--	General Purpose or Port 80, freely configurable*
	green	--	BIOS POST bit 0 and bit 4	
	amber	--	--	

* For further information on configuring the General Purpose LEDs, refer to Chapter 4.4.13, LED Configuration Register, and Chapter 4.4.14, LED Control Register.

Note ...

The bit allocation for Port 80 is the same as for the POST code.

How to Read the 8-Bit POST Code / Port 80

Due to the fact that only 4 bits are available and 8 bits must be displayed, the General Purpose LEDs are multiplexed.

The following table indicates the General Purpose LEDs' operation if BIOS POST/Port 80 configuration is enabled (see also Table 2-9, "General Purpose LED Function").

Table 2-10: POST Code / Port 80

STATE	GENERAL PURPOSE LEDs
0	All LEDs are OFF; start of sequence
1	High nibble
2	Low nibble

Note ...

The output of the POST code is indicated by the General Purpose LEDs on the front panel according to the following sequence:

OFF, high nibble, low nibble, OFF ... (state 0, state 1, state 2, state 0 ...)

Note ...

Under normal operating conditions, the General Purpose LEDs should not remain lit during boot-up. They are intended to be used only for debugging purposes. In the event that a General Purpose LED lights up during boot-up and the CP6001 does not boot, please contact Kontron for further assistance.

2.3.2 USB Interfaces

The CP6001 supports seven USB 2.0 ports (two on the front I/O, one onboard for the USB NAND Flash module, and four on the rear I/O). On the four rear I/O ports it is strongly recommended to use a cable below 3 metres in length for USB 2.0 devices. All seven ports are high-speed, full-speed, and low-speed capable. High-speed USB 2.0 allows data transfers of up to 480 Mb/s.

One USB peripheral may be connected to each port. For connecting more USB devices to the board than there are available ports, an external USB hub is required.

Note ...

The USB host interfaces can be used with maximum 500 mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short-circuit protection is provided. All the signal lines are EMI-filtered.

2.3.2.1 Front Panel USB Connectors J9 and J10

The CP6001 has two USB 2.0 interfaces implemented as 4-pin, type A USB connectors with the following pinout:

Figure 2-1: USB Con. J9 and J10

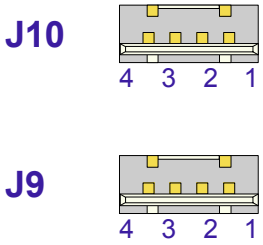


Table 2-11: USB Con. J9 and J10 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	VCC	VCC	--
2	UV0-	Differential USB-	I/O
3	UV0+	Differential USB+	I/O
4	GND	GND	--

Note ...

Windows kernel debugging is supported via the USB Port 0 of the ICH7R chipset. The chipset's USB Port 0 is routed to the front panel USB connector J10.

2.3.2.2 Onboard USB NAND Flash Connector J19

The CP6001 has one onboard USB interface implemented on a 10-pin connector with the following pinout.

Figure 2-2: USB NAND Flash Con. J19

Table 2-12: USB NAND Flash Con. J19 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	VCC	VCC	--
3	UV0-	Differential USB-	I/O
5	UV0+	Differential USB+	I/O
7	GND	GND	--
9	Key		
2, 4, 6, 8	NC	Not connected	--
10	Res.	Reserved	--

2.3.3 Graphics Controller

The 945GM Express GMCH includes a highly integrated graphics accelerator delivering high-performance 3D, 2D graphics capabilities.

The internal graphics controller has two independent display pipes allowing for support of two independent display screens.

Integrated 2D/3D Graphics:

- Intel® Gen3.5 integrated graphics engine
- Smart 2D Display Technology (S2DDT)
- Dynamic Video Memory Technology 3.0 (DVMT)
- Integrated 400 MHz RAMDAC
- Resolution up to 2048 x 1536 pixels @ 75 Hz (QXGA)
- Integrated H/W Motion Compensation for MPEG2 decode

Graphics Memory Usage

The 945GM Express GMCH supports the Dynamic Video Memory Technology (DVMT 3.0). This technology ensures the most efficient use of all available memory for maximum 3D graphics performance. DVMT dynamically responds to application requirements allocating display and texturing memory resources as required.

The graphics controller is fed with data from the 945GM memory controller. The graphics performance is directly related to the amount of memory bandwith available.

Graphics Resolution

The 945GM Express GMCH has an integrated 400 MHz RAMDAC that can directly drive a progressive scan analog monitor up to a resolution of 2048 x 1536 pixels @ 75 Hz.

Graphics Interfaces

The internal graphics controller provides two SDVO interfaces and one analog VGA interface.

The SDVO interfaces support one HDMI interface and one DVI interface via a Transition Minimized Differential Signaling (TMDS) transmitter. The HDMI and DVI interfaces are provided only on rear I/O. In addition, the HDMI interface provides an embedded audio stream that can be decoded by a respective device.

The analog VGA interface is provided on the front panel and is switchable to rear I/O in the BIOS.

The CP6001 allows for the simultaneous connection of three panels to the board. However, only two panels can be active at the same time. This type of connection is known as independent dual-head connection.

Analog VGA Connector J11

The 15-pin female connector, J11, is used to connect an analog VGA monitor to the CP6001.

Figure 2-3: D-Sub VGA Con. J11

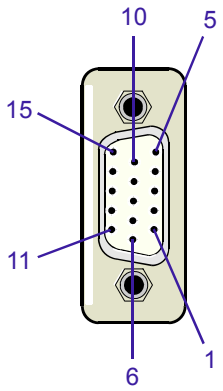


Table 2-13: D-Sub VGA Connector J11 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	Red	Red video signal output	O
2	Green	Green video signal output	O
3	Blue	Blue video signal output	O
10*	VGA_DETECT	Monitor detection signal	I
13	Hsync	Horizontal sync.	TTL Out
14	Vsync	Vertical sync.	TTL Out
12	Sdata	I^2C data (EDID)	I/O
15	Sclk	I^2C clock (EDID)	I/O
9	VCC	Power +5V, 1.5 A fuse protection	O
5,6,7,8	GND	Ground signal	--
4,11	NC	--	--

* Pin 10 is normally defined as Ground but is used on the CP6001 as detection signal of a connected monitor if the BIOS setting for the CP6001 is “AUTO” (the BIOS default setting is “FRONT”).

Note ...

If the automatic VGA detection mechanism on the CP6001 is used, the user must ensure that the VGA cable and the connected monitor have a Ground signal on pin 10. Otherwise the interface is not operable.

2.3.4 COM Ports

The CP6001 provides two COM ports: COM1, which is available on the front panel as a serial RS-232, RJ-45 connector and is routed to rear I/O, and COM2, which is only available as an RS-422 interface on the rear I/O.

COM1 and COM2 are fully compatible with the 16550 controller. The front I/O COM1 port includes a sub-set of handshaking and modem control signals. The rear I/O COM1 port includes a complete set of handshaking and modem control signals. The COM1 and COM2 ports provide maskable interrupt generation. The data transfer on the COM ports is up to 115.2 kbit/s.

The following figure and table provide pinout information for the serial connector J12 (COM1).

Figure 2-4: Serial Con. J12 (COM1)

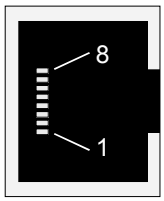


Table 2-14: Serial Con. J12 (COM1) Pinout

PIN	SIGNAL	FUNCTION	I/O
1	RTS	Request to send	O
2	DTR (TX_IPMI)*	Data terminal ready	O
3	TXD	Transmit data	O
4	GND	Signal ground	--
5	GND	Signal ground	--
6	RXD	Receive data	I
7	DSR (RX_IPMI)*	Data set ready	I
8	CTS	Clear to send	I

* The signals marked with a * are multiplexed for IPMI debugging purposes. For further information on the COM port routing, refer to Chapter 4.5.2, IPMI Controller Configuration Register, Table 4-25 in this manual.

2.3.5 Gigabit Ethernet

The CP6001 provides three 10Base-T/100Base-TX/1000Base-T Gigabit Ethernet interfaces on the front panel, two of which are switchable to rear I/O (GbE A and GbE B) in accordance with the PICMG 2.16 specification.

The Gigabit Ethernet interfaces on the CP6001 are based on the Intel® 82573L Gigabit Ethernet controllers, which are connected to the PCI Express interface. The Intel® 82573L Gigabit Ethernet Controller's architecture is optimized to deliver high-performance with the lowest power consumption. The controller's architecture includes independent transmit and receive queues and a PCI Express interface that maximizes the use of bursts for efficient bus usage. The Boot from LAN feature is supported.

The Ethernet connectors J6, J7 and J8 are realized as RJ-45 connectors. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto MDI-X).

Figure 2-5: Gigabit Ethernet Con. J6, J7 and J8

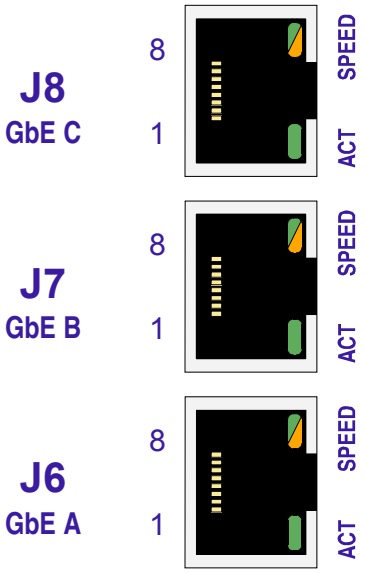


Table 2-15: Pinout of GbE Con. J6, J7 and J8

PIN	MDI / STANDARD ETHERNET CABLE					
	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-	-	I/O	BI_DC+
5	-	-	-	-	I/O	BI_DC-
6	I	RX-	I	RX-	I/O	BI_DB-
7	-	-	-	-	I/O	BI_DD+
8	-	-	-	-	I/O	BI_DD-

Ethernet LED Status

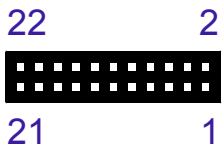
ACT (green): This LED monitors network connection and activity. When this LED is lit, it means that a link has been established. The LED blinks when network packets are sent or received through the RJ-45 port. When this LED is not lit, there is no link established.

SPEED (green/orange): This LED lights up to indicate a successful 100Base-TX or 1000Base-T connection. When green it indicates a 100Base-TX connection and when orange it indicates a 1000Base-TX connection. When not lit and the ACT-LED is active, the connection is operating at 10Base-T.

2.3.6 Extension Connector J14

The I/O extension connector provides cost-effective and flexible configuration options. To provide flexible configuration of additional low-speed PC devices, such as Super I/O, IPMI or CAN controller, the LPC port is connected to the I/O extension connector. The I/O extension interface contains all the signals necessary to connect up to two LPC devices. If the application requires use of this interface, please contact Kontron for further assistance.

Figure 2-6: Extension Con. J14



2.3.7 Serial ATA Interface

The CP6001 provides four Serial ATA (SATA) interfaces: two interfaces implemented as onboard SATA connectors which are switchable to rear I/O, and two SATA interfaces only on the rear I/O. The onboard SATA interfaces support SATA I (1.5 Gbit/sec) and SATA II (3.0 Gbit/sec). One of the onboard SATA connectors supports the mounting of an onboard 2.5" HDD. The other SATA connector is used for standard SATA devices with cable connections.

All SATA interfaces are realized as SATA II with a data transmission with up to 300 MB/s and are compatible with SATA I.

2.3.7.1 Serial ATA Connector J18

The CP6001 provides a SATA connector, J18, which is used to connect standard HDDs and other SATA devices to the CP6001. This SATA channel can be switched either to the SATA Connector J18 or to the rear I/O Connector J5 via the BIOS.

Figure 2-7: SATA Con. J18

Table 2-16: SATA Connector J18 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	GND	Ground signal	--
2	SATA_TX0+	Differential Transmit +	O
3	SATA_TX0-	Differential Transmit -	O
4	GND	Ground signal	--
5	SATA_RX0-	Differential Receive -	I
6	SATA_RX0+	Differential Receive +	I
7	GND	Ground signal	--

Note ...

If the onboard SATA connector, J18, will be used, due to the big SATA connector and the stiff SATA cable, the CP6001 will exceed the thickness of 4HP.

Note ...

To ensure secure connectivity, the SATA connector supports the use of SATA II cables (SATA cables with locking latch).

2.3.7.2 2.5" SATA HDD Extension Connector J20

The CP6001 provides one 12-pin, female SATA extension connector, J20. This connector is used only on the R1 version and serves for connecting an onboard 2.5" Serial ATA HDD to the board through the CP6001-EXT-SATA module. For further information regarding this module, refer to Appendix A.

Figure 2-8: SATA Ext. Con. J20

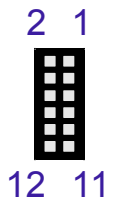
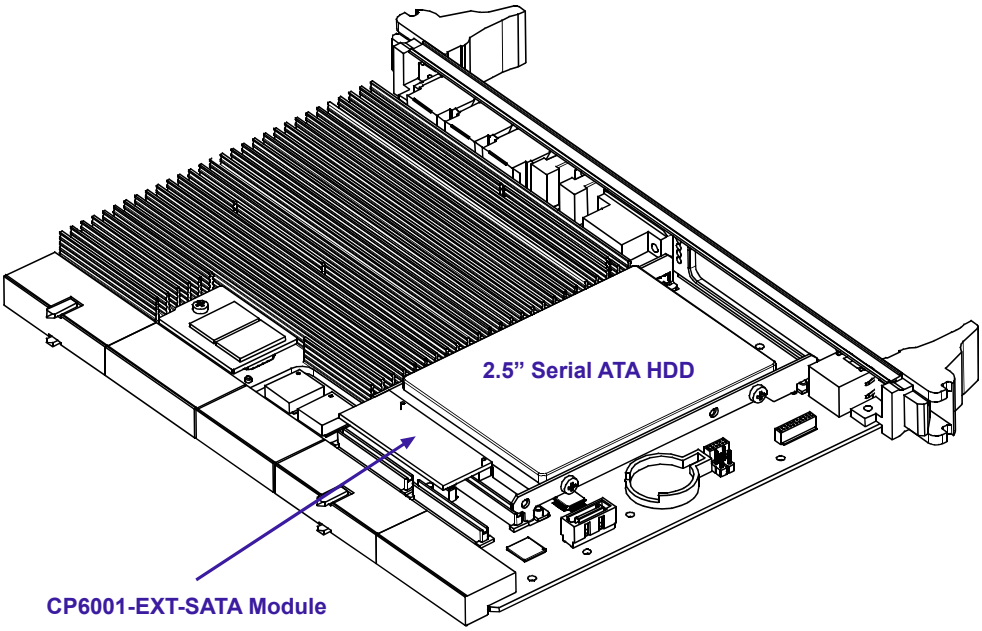


Table 2-17: SATA Extension Connector J20 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	SATA_RX2-	Differential Receive -	I
2	GND	Ground signal	--
3	SATA_RX2+	Differential Receive +	I
4	GND	Ground signal	--
5	GND	Ground signal	--
6	5V	5V power	--
7	SATA_TX2-	Differential Transmit -	O
8	GND	Ground signal	--
9	SATA_TX2+	Differential Transmit +	O
10	GND	Ground signal	--
11	GND	Ground signal	--
12	5V	5V power	--

Figure 2-9: Connecting an Onboard 2.5" SATA HDD to the CP6001-EXT-SATA Module



Note ...

If a CP6001-EXT-SATA module is installed on the CP6001, it is not possible to install a PMC module on the board, and vice versa.

2.3.8 PMC Interface

For flexible and easy configuration one onboard PMC socket is available. The J21 (Jn1) and J23 (Jn2) connectors provide the signals for the 32-bit PCI/PCI-X Bus. User-defined I/O signals are supported on J22 (Jn4) and are connected to the CompactPCI rear I/O connector J4.

This interface has been designed to comply with the IEEEP1386.1 specification, which defines a PCI electrical interface for the CMC (Common Mezzanine Card) form factor. The CP6001 provides 3.3V PMC PCI signaling environment. If 5V PMC PCI signaling environment is required, please contact Kontron for further assistance.

The R1 version allows installing a PMC module on the board. The R2 version allows installing a CCPMC module without front I/O on the board.

Note ...

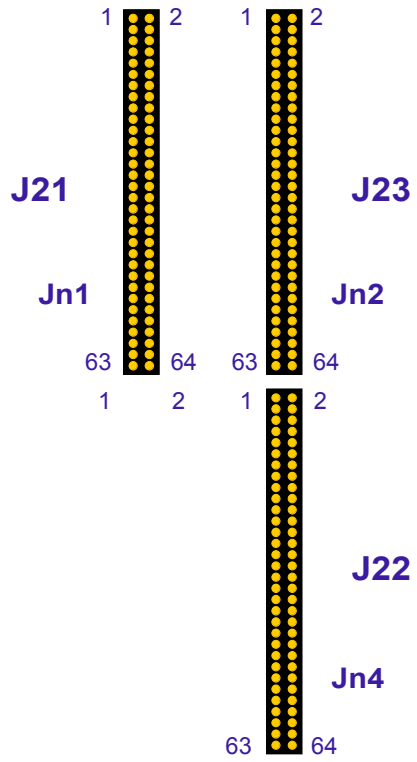
If a PMC module is installed on the CP6001, it is not possible to install a CP6001-EXT-SATA module on the board, and vice versa.

The PMC interface supports the following configurations:

Table 2-18: Onboard PCI Configuration

SIZE	SPEED	INTERFACE
32-bit	33 MHz	PCI
32-bit	66 MHz	PCI/PCI-X

Figure 2-10: PMC Connectors J21, J22 and J23



2.3.8.1 PMC Connectors J21, J22 and J23 Pinouts

Table 2-19: PMC Connectors J21 and J23 Pinouts

J21 (Jn1)				J23 (Jn2)			
SIGNAL	PIN	PIN	SIGNAL	SIGNAL	PIN	PIN	SIGNAL
TCK (pull-up)	1	2	-12V	+12V	1	2	TRST# (pull-down)
Ground	3	4	INTA#	TMS (pull-up)	3	4	TDO (NC)
INTB#	5	6	INTC#	TDI (pull-up)	5	6	Ground
BUSMODE1# (NC)	7	8	+5V	Ground	7	8	PCI-RSV (NC)
INTD#	9	10	PCI-RSV (NC)	PCI-RSV (NC)	9	10	PCI-RSV (NC)
Ground	11	12	3V3-AUX (NC)	BUSMODE2# (pull-up)	11	12	+3.3V
CLK	13	14	Ground	RST#	13	14	BUSMODE3# (GND)
Ground	15	16	GNT#	+3.3V	15	16	BUSMODE4# (GND)
REQ#	17	18	+5V	PME# (pull-up)	17	18	Ground
V (I/O)	19	20	AD[31]	AD[30]	19	20	AD[29]
AD[28]	21	22	AD[27]	Ground	21	22	AD[26]
AD[25]	23	24	Ground	AD[24]	23	24	+3.3V
Ground	25	26	C/BE[3]	IDSEL	25	26	AD[23]
AD[22]	27	28	AD[21]	+3.3V	27	28	AD[20]
AD[19]	29	30	+5V	AD[18]	29	30	Ground
V (I/O)	31	32	AD[17]	AD[16]	31	32	C/BE[2]#
FRAME#	33	34	Ground	Ground	33	34	PMC-RSV (NC)
Ground	35	36	IRDY#	TRDY#	35	36	+3.3V
DEVSEL#	37	38	+5V	Ground	37	38	STOP#
PCIXCAP (GND)	39	40	LOCK#	PERR#	39	40	Ground
PCI-RSV (NC)	41	42	PCI-RSV (NC)	+3.3V	41	42	SERR#
PAR	43	44	Ground	C/BE[1]#	43	44	Ground
V (I/O)	45	46	AD[15]	AD[14]	45	46	AD[13]
AD[12]	47	48	AD[11]	M66EN	47	48	AD[10]
AD[09]	49	50	+5V	AD[08]	49	50	+3.3V
Ground	51	52	C/BE[0]#	AD[07]	51	52	PMC-RSV (NC)
AD[06]	53	54	AD[05]	+3.3V	53	54	PMC-RSV (NC)
AD[04]	55	56	Ground	PMC-RSV (NC)	55	56	Ground
V (I/O)	57	58	AD[03]	PMC-RSV (NC)	57	58	PMC-RSV (NC)
AD[02]	59	60	AD[01]	Ground	59	60	PMC-RSV (NC)
AD[00]	61	62	+5V	ACK64#	61	62	+3.3V
Ground	63	64	REQ64#	Ground	63	64	PMC-RSV (NC)

Note ...

The PMC capabilities are detected using the REQ64# and M66EN signals.
The host controller detects the bus speed via the M66EN signal.
Low: PCI 33 MHz; High: PCI 66 MHz

Table 2-20: PMC Connectors J22 Pinout

J22 (Jn4)			
SIGNAL	PIN	PIN	SIGNAL
Rear I/O+	1	2	Rear I/O+
Rear I/O-	3	4	Rear I/O-
Rear I/O+	5	6	Rear I/O+
Rear I/O-	7	8	Rear I/O-
Rear I/O+	9	10	Rear I/O+
Rear I/O-	11	12	Rear I/O-
Rear I/O+	13	14	Rear I/O+
Rear I/O-	15	16	Rear I/O-
Rear I/O+	17	18	Rear I/O+
Rear I/O-	19	20	Rear I/O-
Rear I/O+	21	22	Rear I/O+
Rear I/O-	23	24	Rear I/O-
Rear I/O+	25	26	Rear I/O+
Rear I/O-	27	28	Rear I/O-
Rear I/O+	29	30	Rear I/O+
Rear I/O-	31	32	Rear I/O-
Rear I/O+	33	34	Rear I/O+
Rear I/O-	35	36	Rear I/O-
Rear I/O+	37	38	Rear I/O+
Rear I/O-	39	40	Rear I/O-
Rear I/O+	41	42	Rear I/O+
Rear I/O-	43	44	Rear I/O-
Rear I/O+	45	46	Rear I/O+
Rear I/O-	47	48	Rear I/O-
Rear I/O+	49	50	Rear I/O+
Rear I/O-	51	52	Rear I/O-
Rear I/O+	53	54	Rear I/O+
Rear I/O-	55	56	Rear I/O-
Rear I/O+	57	58	Rear I/O+
Rear I/O-	59	60	Rear I/O-
Rear I/O+	61	62	Rear I/O+
Rear I/O-	63	64	Rear I/O-

The signals from the J22 (Jn4) PMC connector are routed to the J4 CompactPCI rear I/O connector in such a way that they can behave as differential signal pairs. The paired signals are indicated by shading in the table above.

For example, the pathways from pins 1 and 3 are physically routed on the board as a pair to the J4 rear I/O connector. Thus, they can be used for a differential signal pair.

2.3.9 Debug Interface

For hardware and software debugging, the CP6001 provides four bicolor General Purpose LEDs (LED0..3), which indicate hardware failures, the BIOS POST codes and the Port 80 user-configurable outputs.

2.3.10 CompactPCI Interface

The CP6001 supports a flexibly configurable, hot swap CompactPCI interface. In the System Master slot the interface is in the transparent mode, and in the peripheral slot the CompactPCI interface is isolated so that it cannot communicate with the CompactPCI bus. This mode is known as "passive mode".

2.3.10.1 System Master Configuration

In a system slot, the CP6001 can communicate with all other CompactPCI boards through a 32-bit/66 MHz interface.

The CP6001 supports up to seven CompactPCI loads through a backplane and is fully compliant with the PCI Local Bus Specification Rev. 2.3 for 32-bit/66 MHz.

2.3.10.2 Peripheral Master Configuration (Passive Mode)

In a peripheral slot, the board receives power but does not communicate on the CompactPCI bus; all CompactPCI signals are isolated.

In this configuration, the communication can be achieved via the two Gigabit Ethernet ports as defined in the PICMG 2.16 specification.

2.3.10.3 Packet Switching Backplane (PICMG 2.16)

The CP6001 supports a dual Gigabit Ethernet link port (Node) on the J3 connector in accordance with the CompactPCI Packet Switching Backplane Specification PICMG 2.16, Version 1.0. The two nodes are connected in the chassis via the CompactPCI Packet Switching Backplane to the Fabric slots "A" and "B".

The PICMG 2.16 feature can be used in the system slot and in the peripheral slot. In order to use this feature, the GbE A (J6) and GbE B (J7) Gigabit Ethernet ports must be switched to rear I/O in the BIOS.

2.3.10.4 Hot Swap Support

To ensure that a board may be removed and replaced in a working bus without disturbing the system, the following additional features are required:

- Power ramping
- Precharge
- Hot swap control and status register bits
- Automatic interrupt generation whenever a board is about to be removed or replaced
- An LED to indicate that the board may be safely removed

2.3.10.5 Power Ramping

On the CP6001 a special hot swap controller is used to ramp up the onboard supply voltage. This is done to avoid transients on the +3.3V, +5V, +12V and -12V power supplies from the hot swap system. When the power supply is stable, the hot swap controller generates an onboard reset to put the board into a definite state.

2.3.10.6 Precharge

Precharge is provided on the CP6001 by a resistor on each signal line (PCI bus), connected to a +1V reference voltage. If the board is configured in the system master configuration, the reference voltage is disabled.

2.3.10.7 Handle Switch

A microswitch is situated in the extractor handle. The status of the handle is included in the onboard logic. The microswitch is connected to the onboard connector J13.

2.3.10.8 ENUM# Interrupt

In system master configuration the ENUM signal is an input.

2.3.10.9 Hot Swap LED

On the CP6001 the is controlled via IPMI and indicates when the shutdown process is finished and the board is ready for extraction.

2.3.11 CompactPCI Bus Connector

The complete CompactPCI connector configuration comprises five connectors named J1 to J5. Their functions are as follows:

- J1/J2: 64-bit CompactPCI interface with PCI bus signals, arbitration, clock and power
- J3, J4 and J5 have rear I/O interface functionality
- J4 only has optional rear I/O functionality from the PMC module

The CP6001 is designed for a CompactPCI bus architecture. The CompactPCI standard is electrically identical to the PCI local bus. However, these systems are enhanced to operate in rugged industrial environments and to support multiple slots.

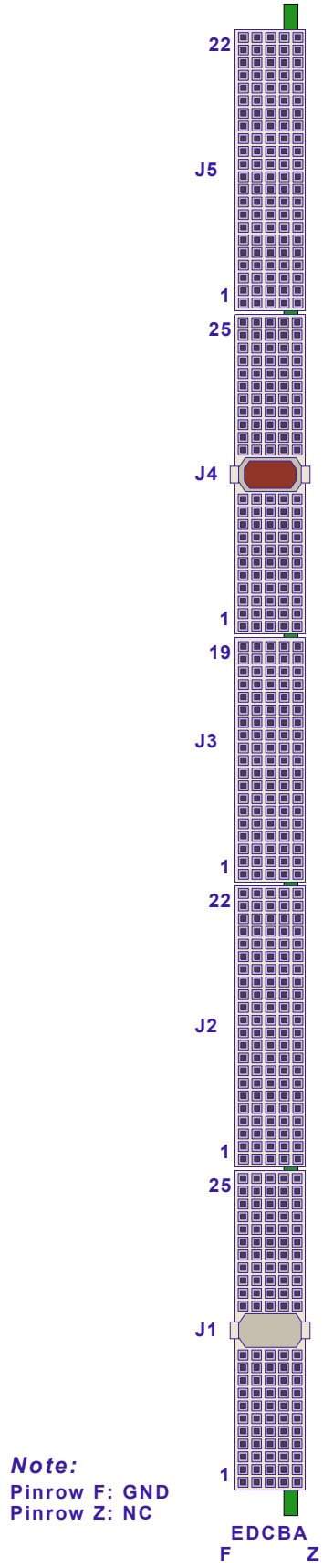
2.3.11.1 CompactPCI Connector Keying

CompactPCI connectors support guide lugs to ensure a correct polarized mating.

To prevent plugging the CP6001 into an H.110 backplane slot, a brown key is installed in J4.

The CP6001 supports universal PCI VI/O signaling voltages with one common termination resistor configuration and includes a PCI VI/O voltage detection circuit. If the PCI VI/O voltage is 5 V, the maximum supported PCI frequency is 33 MHz.

Figure 2-11: CPCI Connectors J1-J5



2.3.11.2 CompactPCI Connectors J1 and J2 Pinouts

The CP6001 is provided with two 2 mm x 2 mm pitch female CompactPCI bus connectors, J1 and J2.

Table 2-21: CompactPCI Bus Connector J1 System Slot Pinout

PIN	Z	A	B	C	D	E	F
25	NC	5V	REQ64#	ENUM#	3.3V	5V	GND
24	NC	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	NC	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	NC	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	NC	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	NC	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	NC	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	NC	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	NC	3.3V	IPMB SCL	IPMB SDA	GND	PERR#	GND
16	NC	DEVSEL#	PCI-X_CAP	V(I/O)	STOP#	LOCK#	GND
15	NC	3.3V	FRAME#	IRDY#	BDSEL#	TRDY#	GND
14-12	Key Area						
11	NC	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	NC	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	NC	C/BE[3]#	NC	AD[23]	GND	AD[22]	GND
8	NC	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	NC	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	NC	REQ0#	CPCI_Present#	3.3V	CLK0	AD[31]	GND
5	NC	RSV	RSV	RST#	GND	GNT0#	GND
4	NC	IPMB PWR	Health#	V(I/O)	RSV	RSV	GND
3	NC	INTA#	INTB#	INTC#	5V	INTD#	GND
2	NC	TCK	5V	TMS	NC	TDI	GND
1	NC	5V	-12V	TRST#	+12V	5V	GND

Table 2-22: CompactPCI Bus Connector J1 Peripheral Slot Pinout

PIN	Z	A	B	C	D	E	F
25	NC	5V	*	ENUM#	3.3V	5V	GND
24	NC	*	5V	V(I/O)	*	*	GND
23	NC	3.3V	*	*	5V	*	GND
22	NC	*	GND	3.3V	*	*	GND
21	NC	3.3V	*	*	M66EN	*	GND
20	NC	*	GND	V(I/O)	*	*	GND
19	NC	3.3V	*	*	GND	*	GND
18	NC	*	GND	3.3V	*	*	GND
17	NC	3.3V	IPMB SCL	IPMB SDA	GND	*	GND
16	NC	*	*	V(I/O)	*	*	GND
15	NC	3.3V	*	*	BDSEL#	*	GND
14-12	Key Area						
11	NC	*	*	*	GND	*	GND
10	NC	*	GND	3.3V	*	*	GND
9	NC	*	NC	*	GND	*	GND
8	NC	*	GND	V(I/O)	*	*	GND
7	NC	*	*	*	GND	*	GND
6	NC	*	CPCI_Present#	3.3V	*	*	GND
5	NC	RSV	RSV	RST#**	GND	*	GND
4	NC	IPMB PWR	Healthy#	V(I/O)	RSV	RSV	GND
3	NC	*	*	*	5V	*	GND
2	NC	TCK	5V	TMS	NC	TDI	GND
1	NC	5V	-12V	TRST#	+12V	5V	GND

Note ...

A * indicates that the signal normally present at this pin is disconnected from the CompactPCI bus when the CP6001 is inserted in a peripheral slot.

** When the CP6001 is inserted in a peripheral slot, the function of the RST# signal is maskable.

Table 2-23: 64-bit CompactPCI Bus Connector J2 System Slot Pinout

PIN	Z	A	B	C	D	E	F
22	NC	GA4	GA3	GA2	GA1	GA0	GND
21	NC	CLK6	GND	RSV	RSV	RSV	GND
20	NC	CLK5	GND	RSV	GND	RSV	GND
19	NC	GND	GND	IPMB2_SDA	IPMB2_SCL	IPMB2_Alert	GND
18	NC	RSV	RSV	RSV	GND	RSV	GND
17	NC	RSV	GND	PRST#	REQ6#	GNT6#	GND
16	NC	RSV	RSV	DEG#	GND	RSV	GND
15	NC	RSV	GND	FAL#	REQ5#	GNT5#	GND
14	NC	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	NC	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND
12	NC	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	NC	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	NC	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	NC	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	NC	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	NC	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	NC	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	NC	C/BE[5]#	NC	V(I/O)	C/BE[4]#	PAR64	GND
4	NC	V(I/O)	RSV	C/BE[7]#	GND	C/BE[6]#	GND
3	NC	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	NC	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	NC	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Table 2-24: 64-bit CompactPCI Bus Connector J2 Peripheral Slot Pinout

PIN	Z	A	B	C	D	E	F
22	NC	GA4	GA3	GA2	GA1	GA0	GND
21	NC	*	GND	RSV	RSV	RSV	GND
20	NC	*	GND	RSV	GND	RSV	GND
19	NC	GND	GND	IPMB2_SDA	IPMB2_SCL	IPMB2_Alert	GND
18	NC	RSV	RSV	RSV	GND	RSV	GND
17	NC	RSV	GND	*	*	*	GND
16	NC	RSV	RSV	DEG#	GND	RSV	GND
15	NC	RSV	GND	FAL#	*	*	GND
14	NC	*	*	*	GND	*	GND
13	NC	*	GND	V(I/O)	*	*	GND
12	NC	*	*	*	GND	*	GND
11	NC	*	GND	V(I/O)	*	*	GND
10	NC	*	*	*	GND	*	GND
9	NC	*	GND	V(I/O)	*	*	GND
8	NC	*	*	*	GND	*	GND
7	NC	*	GND	V(I/O)	*	*	GND
6	NC	*	*	*	GND	*	GND
5	NC	*	NC	V(I/O)	*	*	GND
4	NC	V(I/O)	RSV	*	GND	*	GND
3	NC	*	GND	*	*	*	GND
2	NC	*	*	SYSEN#	*	*	GND
1	NC	*	GND	*	*	*	GND

Note ...

A * indicates that the signal normally present at this pin is disconnected from the CompactPCI bus when the CP6001 is inserted in a peripheral slot.

2.3.11.3 CompactPCI Rear I/O Connectors J3-J5 and Pinouts

The CP6001 board provides optional rear I/O connectivity for peripherals. All standard PC interfaces are implemented and assigned to the front panel and to the rear I/O connectors J3, and J5.

When the rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus, the rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For the system rear I/O feature a special backplane is necessary. The CP6001 with rear I/O is compatible with all standard 6U CompactPCI passive backplanes with rear I/O support.

The CP6001 conducts all I/O signals through the rear I/O connectors J3, J4 and J5.

Table 2-25: CompactPCI Rear I/O Connector J3 Pinout

PIN	Z	A	B	C	D	E	F
19	NC	RIO_VCC	RIO_VCC	RIO_3.3V	RIO_+12V	RIO_-12V	GND
18	NC	LPa_DA+	LPa_DA-	GND	LPa_DC+	LPa_DC-	GND
17	NC	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-	GND
16	NC	LPb_DA+	LPb_DA-	GND	LPb_DC+	LPb_DC-	GND
15	NC	LPb_DB+	LPb_DB-	GND	LPb_DD+	LPb_DD-	GND
14	NC	LPa:LINK	LPb:LINK	LPab:CT1	RSV	FAN:SENSE2	GND
13	NC	LPa:ACT	LPb:ACT	RSV	RSV	FAN:SENSE1	GND
12	NC	RSV	RSV	GND	RSV	RSV	GND
11	NC	RSV	RSV	GND	RSV	RSV	GND
10	NC	USB1:VCC	USB0:VCC	GND	USB3:VCC	USB2:VCC	GND
9	NC	USB1:D-	USB1:D+	GND	USB3:D-	USB3:D+	GND
8	NC	USB0:D-	USB0:D+	GND	USB2:D-	USB2:D+	GND
7	NC	RIO_3.3V	RSV	ID3	ID4	SPEAKER	GND
6	NC	VGA:RED	VGA:GREEN	VGA:SDA	RSV	RSV	GND
5	NC	VGA:BLUE	VGA:HSYNC	VGA:VSYNC	VGA:SCL	PS2:CLK	GND
4	NC	RSV	RSV	SP1:TX-	SP1:TX+	PS2:DATA	GND
3	NC	RSV	RSV	SP1:RX-	SP1:RX+	PS2:DATA	GND
2	NC	SP0:RI	SP0:DTR	SP0:CTS	SP0:TX	PS2:CLK	GND
1	NC	SP0:RTS	SP0:RX	SP0:DSR	SP0:DCD	ID1	GND

Warning!

The RIO_XXX signals are power supply **OUTPUTS** to supply the rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module.

Failure to comply with the above will result in damage to your board.

The following table describes the signals of the J3 connector.

Table 2-26: CompactPCI Rear I/O Connector J3 Signals

SIGNAL	DESCRIPTION
SP0	COM1 Signaling (RS-232)
SP1	COM2 Signaling (RS-422)
VGA	Graphic Signaling
USB0 to USB3	USB Port Signaling
PS2	PS/2 Keyboard / Mouse Signaling
SPEAKER	Standard PC Speaker
FAN	Fan Sensoring
LPa	Rear I/O LAN Port B
LPb	Rear I/O LAN Port A

Table 2-27: CompactPCI Rear I/O Connector J4 Pinout

PIN	Z	A	B	C	D	E	F
25	NC	PIM:1	PIM:3	GND	PIM:2	PIM:4	GND
24	NC	PIM:5	PIM:7	GND	PIM:6	PIM:8	GND
23	NC	NC	RIO_VCC	GND	NC	RIO_3.3V	GND
22	NC	PIM:9	PIM:11	GND	PIM:10	PIM:12	GND
21	NC	PIM:13	PIM:15	GND	PIM:14	PIM:16	GND
20	NC	GND	GND	GND	GND	GND	GND
19	NC	PIM:17	PIM:19	GND	PIM:18	PIM:20	GND
18	NC	PIM:21	PIM:23	GND	PIM:22	PIM:24	GND
17	NC	GND	GND	GND	GND	GND	GND
16	NC	PIM:25	PIM:27	GND	PIM:26	PIM:28	GND
15	NC	PIM:29	PIM:31	GND	PIM:30	PIM:32	GND
14 -12	Key Area						
11	NC	PIM:33	PIM:35	GND	PIM:34	PIM:36	GND
10	NC	PIM:37	PIM:39	GND	PIM:38	PIM:40	GND
9	NC	GND	GND	GND	GND	GND	GND
8	NC	PIM:41	PIM:43	GND	PIM:42	PIM:44	GND
7	NC	PIM:45	PIM:47	GND	PIM:46	PIM:48	GND
6	NC	GND	GND	GND	GND	GND	GND
5	NC	PIM:49	PIM:51	GND	PIM:50	PIM:52	GND
4	NC	PIM:53	PIM:55	GND	PIM:54	PIM:56	GND
3	NC	GND	GND	GND	GND	GND	GND
2	NC	PIM:57	PIM:59	GND	PIM:58	PIM:60	GND
1	NC	PIM:61	PIM:63	GND	PIM:62	PIM:64	GND

The signals from the J4 CompactPCI rear I/O connector are routed to the J22 (Jn4) PMC connector in such a way that they can behave as differential signal pairs. The paired signals are indicated by shading in the table above.

For example, the pathways from pins A1 and B1 are physically routed on the board as a pair to the J22 (Jn4) PMC connector. Thus, they can be used for a differential signal pair.

Table 2-28: CompactPCI Rear I/O Connector J5 Pinout

PIN	Z	A	B	C	D	E	F
22	NC	SATA:LED	PWM1:OUT	GND	PWM2:OUT	BATT (3.0V)	GND
21	NC	HDA:SYNC	HDA:RST	GND	HDA:SDOUT	SYS_WP#	GND
20	NC	GPIO0	HDA:SDIN1	GND	GPIO1	HDA:SDIN2	GND
19	NC	GND	GND	GND	HDA:SDIN0*	HDA:BITCLK	GND
18	NC	DVI2:D0+	DVI2:D0-	GND	GND	GND	GND
17	NC	DVI2:D2+	DVI2:D2-	GND	DVI2:D1+	DVI2:D1-	GND
16	NC	RSV	DVI2:HPDET	GND	RSV	RSV	GND
15	NC	DVI2:CLK+	DVI2:CLK-	GND	DVI2:SDA	DVI2:SDC	GND
14	NC	GND	GND	GND	GND	GND	GND
13	NC	DVI1:D0+	DVI1:D0-	GND	DVI1:D1+	DVI1:D1-	GND
12	NC	DVI1:D2+	DVI1:D2-	GND	RSV	RSV	GND
11	NC	RSV	DVI1:HPDET	GND	DVI1:SDA	DVI1:SDC	GND
10	NC	DVI1:CLK+	DVI1:CLK-	GND	SMB:SDA	SMB:SCL	GND
9	NC	GND	GND	GND	GND	GND	GND
8	NC	HT3:TX+	HT3:TX-	GND	HT3:RX+	HT3:RX-	GND
7	NC	GND	GND	GND	GND	GND	GND
6	NC	HT2:TX+	HT2:TX-	GND	HT2:RX+	HT2:RX-	GND
5	NC	GND	GND	GND	GND	GND	GND
4	NC	HT1:TX+	HT1:TX-	GND	HT1:RX+	HT1:RX-	GND
3	NC	GND	GND	GND	GND	GND	GND
2	NC	HT0:TX+	HT0:TX-	GND	HT0:RX+	HT0:RX-	GND
1	NC	GND	GND	GND	GND	GND	GND

* The HDA:SDIN0 signal (D19) is not available because the HDMI TMDS transmitter uses it for the internal audio codec.

The following table describes the signals of the J5 connector.

Table 2-29: CompactPCI Rear I/O Connector J5 Signals

SIGNAL	DESCRIPTION
HT0..HT3	SATA Port 0..3 Signaling
SMB	System Management Bus Signaling
DVI1	HDMI signaling
DVI2	DVI signaling
HDA	High-definition audio signaling
PWM	Pulse width modulation output for fan
SATA	Serial ATA LED signaling
GPIO	General purpose digital input/output
SYS_WP#	System write protection for non-volatile memory devices
BATT (3.0V)	Back-up power input for RTC and CMOS RAM

2.3.11.4 Rear I/O Configuration

Rear I/O interfaces are only available on the rear I/O version of the board.

Ethernet Interfaces

Gigabit Ethernet signals are available on the front panel connector and on the rear I/O interface (PICMG 2.16 pinout). It is not possible to operate both the rear and front I/O at the same time. Switching over from the front to rear I/O or vice versa is effected under BIOS control without the need to plug/unplug the Ethernet cables.

Graphics interface

The CP6001 allows for the simultaneous connection of three panels to the board. However, only two panels can be active at the same time. This type of connection is known as independent dual-head connection.

Serial Interfaces COM1 and COM2

For COM1 only one interface may be used (rear I/O or front I/O). COM2 is available only on rear I/O.

Keyboard/Mouse Interface

The keyboard/mouse interface is only available via the rear I/O.

USB Interface

Four USB interfaces are available via the rear I/O. The USB power comes from the baseboard and it is protected by a self-resettable fuse.

SATA

The SATA0 and SATA2 interfaces are available onboard and can be switched to rear I/O. The SATA1 and SATA3 interfaces are available only on rear I/O. Please contact Kontron for further information regarding the SATA0 to SATA3 interface constraints, especially when designing a backplane.

PMC Rear I/O

The PMC rear I/O pinout is optimized to connect the Kontron SCSI PMC board (PMC 261). This module provides SCSI rear I/O support. Other PMC modules with rear I/O functionality can also be used on the CP6001.

2.4 Intelligent Platform Management Interface

2.4.1 Technical Background of IPMI

The CP6001 has been designed to support the "Intelligent Platform Management Interface" (IPMI) subsystem which is another step in providing high-availability platforms. Intelligent Platform Management means monitoring the health of the entire system beyond the confines of the board itself, so that the status of the complete system is available to be used, for example, for control and intervention purposes. A range of variables is monitored on every board, to provide information on the system status, e.g. voltages, temperature, powergood signals, reset signals etc. Additionally, the IPMI Baseboard Management Controller can intervene, regulating the operating status of the system by controlling fans, shutting down systems and generating alarm signals as and when fault conditions occur. These fault conditions are simultaneously logged in non-volatile memory for analysis and for fault recovery. IPMI also defines a protocol (software stack) for exchanging the status messages of the board, so that "IPMI ready" boards/systems from different suppliers can be monitored. In addition, a clear interface (registers, addresses etc.) is defined for guaranteeing that System Management software can work with every compliant IPMI hardware.

The electrical interconnection between IPMI capable boards is an I²C interface (IPMB). In CompactPCI systems, this interface is provided on IPMI prepared backplanes and guarantees the data path between the boards.

The devices which handle the measurements and the protocol stack are microcontrollers known as Baseboard Management Controller (BMC), and Peripheral Management Controller (PM) or Satellite Management Controller (SMC). The entire IPMI protocol is controlled by the BMC. On the CP6001, the IPMI controller can be configured to act as BMC or PM/SMC.

The interface between the system controller CPU's System Management software and the Baseboard Management Controller is realized as a keyboard controller style interface (KCS) which can be found in the board's I/O space.

2.4.2 IPMI Glossary

BMC	Baseboard Management Controller In a CompactPCI chassis, there can be only one BMC present.
BT	Block Transfer Interface
FRU	Field Replaceable Units A FRU is available in BMC or satellite mode.
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
KCS	Keyboard Controller Style
PM	Peripheral Management Controller The PM is a microcontroller located on the peripheral board in a Compact-PCI system and handles the measurements and the protocol stack.
SDR	Sensor Data Record
SDRR	Sensor Data Record Repository The SDRR is only present in the BMC. Normally, the SDRR contains all sensor records of the chassis.
SEL	System Event Log The SEL repository is present only in the BMC.
SMC	Satellite Management Controller Slave mode of BMC
SMS	System Management Software

2.4.3 IPMI Implementation on the CP6001

This product fully supports the Intelligent Platform Management Interface v1.5 and PICMG 2.9 R1.0 specifications. It uses a 16-bit micro-controller (Hitachi H8/2166) to run an IPMI firmware. All the information collected by the IPMI controller is then accessible by software through a keyboard-style Interface (see IPMI - Intelligent Platform Management Interface Specification v1.5 for more information).

Features of the IPMI implemented on the CP6001:

- Compliant with PICMG 2.9 specification
- Firmware designed and specially made for CompactPCI implementation
- KCS SMS interface with interrupt support
- Dual Port IPMB configurable as two independent channels or in redundant mode
- Comprehensive set of threshold and discrete sensors
- Sensor thresholds fully configurable
- Complete IPMI watchdog functionality (reset, power down, power cycle)
- Complete SEL, SDRR and FRU functionality
- Master Read/Write I²C support for external I²C communication devices (FRU, EEPROM, FAN)
- FRU data capacity: 4KB
- BMC Firmware can be updated in field under Linux using the free tool 'ipmitool' (http://ipmitool.sourceforge.net)
- Firmware customizable according to the customer needs via BIOS (BMC in SMC operation mode)
- Interoperable with other IPMI solution
- Firmware Hub Flash selection by IPMI OEM command
- Boot order configuration by IPMI OEM command
- POST code reading
- Geographic address support
- Payload power control
- Two fan speed inputs
- Hot swap LED
- Hot swap controller
- Board reset

2.4.3.1 Sensors Implemented on the CP6001

The IPMI firmware includes many sensors. The CP6001 implements several sensors, such as sensors for voltage and pass/fail type signal monitoring. Each sensor's description is built in the IPMI firmware and is accessible to the SMS.

The following tables indicate the sensors implemented on the CP6001.

Table 2-30: Processor, Chipset and General Board Supervision

FUNCTION	DESCRIPTION
Post Value	Post value from host I/O port 80h
FWH0 Boot Error	Firmware Hub 0 boot error
FWH1 Boot Error	Firmware Hub 1 boot error
CPU status	Supports the 'Thermal Trip' bit
Health error	Aggregate state for power error, temperature error etc.
Board reset	Indicates the cause of the last reset
Critical interrupt: NMI	Status of processor NMI line
Critical interrupt: SMI	Timeout during SMI processing
HW Logic index	Index of hardware and logic device (refer to Chapter 4.4.9, Board and PLD Revision Register, Table 4-16)

Table 2-31: Various BMC/SMC Sensors

FUNCTION	DESCRIPTION
Storage error	Indicates a memory error in the BMC subsystem
IPMB 0 stuck	Error on IPMB 0 (cable, interconnect)
IPMB 1 stuck	Error on IPMB 1 (cable, interconnect)
Init agent error	Only present on BMC. Reports initialization problems, e.g. inconsistent SDRR
Watchdog	IPMI Watchdog states
BMC/SMC reboot	Indicates the current reboot of BMC/SMC

Table 2-32: CompactPCI Sensors

FUNCTION	DESCRIPTION
System slot detection	Indicates board is in a system slot
Backplane power supply	Status of power supply, OEM sensor reading includes the BDSEL monitoring
Backplane BDSEL	Refer to the backplane power supply and/or application documentation.
Hot Swap handle	Status of hot swap handle

Table 2-33: Onboard Power Supply Supervision

FUNCTION	DESCRIPTION
Power good	Statuses of all power lines
Power good event	Power fail events for all power lines

Table 2-34: Onboard Voltage Sensors

FUNCTION	PRECISION	DESCRIPTION
Voltage 5V	1%	Board 5V supply
Voltage 3.3V	1%	Board 3.3V supply
Voltage IPMI 5V	1%	IPMI 5V supply
Voltage 1.5V	1%	Board 1.5V supply
Voltage 1.8V	1%	Board 1.8V supply
Voltage 0.9V	1%	DDR termination supply
Voltage battery	1%	Board RTC battery

Table 2-35: Temperature Sensors

FUNCTION	DESCRIPTION
Processor temperature	Current processor temperature
Board temperature 1	Current board temperature below the heat sink near the CPU
Board temperature 2	Current board temperature near the BMC
Processor hot	Indicates a CPU overtemperature event (DIE temperature)

Table 2-36: Fan Sense Sensors

FUNCTION	DESCRIPTION
Fan sense 1	Fan tachometer input 1 (rear)
Fan sense 2	Fan tachometer input 2 (rear)

2.4.4 Data Repositories

All the data gathered by the BMC is stored in a non-volatile memory, providing the possibility to obtain information about working conditions and failure situations.

Chapter 3

Installation

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3. Installation

The CP6001 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

3.1 Safety Requirements

The following safety precautions must be observed when installing or operating the CP6001. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.

Caution!

If your board type is not specifically qualified as being hot swap capable, switch off the CompactPCI system power before installing the board in a free CompactPCI slot. Failure to do so could endanger your life or health and may damage your board or system.

Note ...

Certain CompactPCI boards require bus master and/or rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure that your system is provided with an appropriate free slot in which to insert the board.

ESD Equipment!

This CompactPCI board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

3.2 Initial Installation Procedures

The following procedures are applicable only for the initial installation of the CP6001 in a system. Procedures for standard removal and hot swap operations are found in their respective chapters.

To perform an initial installation of both the CP6001 in a system, proceed as follows:

1. Ensure that the safety requirements indicated Chapter 3.1 are observed.

Warning!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the CP6001 refer to Chapter 4. For the installation of CP6001 specific peripheral devices and rear I/O devices refer to the appropriate sections in Chapter 3.

Warning!

Care must be taken when applying the procedures below to ensure that neither the CP6001 nor other system boards are physically damaged by the application of these procedures.

3. To install the CP6001 perform the following:
   1. Ensure that no power is applied to the system before proceeding.

Warning!

Even though power may be removed from the system, the CP6001 front panel cables and, when installed, the RIO transition module front panel cables may have power applied which comes from an external source.

In addition, these cables may be connected to devices that can be damaged by electrostatic discharging or short-circuiting of pins.

It is the responsibility of the system designer or integrator to ensure that appropriate measures are taken to preclude damage to the system or injury to personnel which may arise from the handling of these cables (connecting or disconnecting).

Kontron disclaims all liability for damages or injuries resulting from failure to comply with the above.

Warning!

When performing the next step, **DO NOT** push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

   2. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.

3. Using both ejector handles, engage the board with the backplane. When the ejector handles are locked, the board is engaged.
4. Fasten the two front panel retaining screws.
5. Connect all external interfacing cables to the board as required.
6. Ensure that the board and all required interfacing cables are properly secured.

The CP6001 is now ready for initial operation. Except for the BIOS, at this point there is no other software installed. For software installation and further operation of the CP6001, refer to appropriate CP6001 software (BIOS, BSP, OS), application, and system documentation.

Warning!

During power-up, the 3.3 V input power supply must be able to provide a minimum peak current of 10 A to the CP6001. This applies for each CP6001 in a given system.

Failure to comply with the instruction above may result in damage to or improper operation of the CP6001.

3.3 Standard Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

Warning!

Care must be taken when applying the procedures below to ensure that neither the CP6001 nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.

Warning!

Even though power may be removed from the system, the CP6001 front panel cables and, when installed, the RIO transition module front panel cables may have power applied which comes from an external source.

In addition, these cables may be connected to devices that can be damaged by electrostatic discharging or short-circuiting of pins.

It is the responsibility of the system designer or integrator to ensure that appropriate measures are taken to preclude damage to the system or injury to personnel which may arise from the handling of these cables (connecting or disconnecting).

Kontron disclaims all liability for damages or injuries resulting from failure to comply with the above.

3. Disconnect any interfacing cables that may be connected to the board.

4. Unscrew the front panel retaining screws.

Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when handling the board.

5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.
7. Dispose of the board as required.

3.4 Hot Swap Procedures

The CP6001 is designed for hot swap operation. When installed in the system slot it is capable of supporting peripheral board hot swapping. When installed in a peripheral slot, its hot swap capabilities depend on the type of backplane in use and the system controller's capabilities. The reason for this being that communications with the system controller requires either front panel Ethernet I/O or use of a packet switching backplane. In any event, hot swap is also a function of the application running on the CP6001.

3.4.1 System Master Hot Swap

Hot swapping of the CP6001 itself when used as the system controller is possible, but will result in any event in a cold start of the CP6001 and consequently a reinitialization of all peripheral boards. Exactly what transpires in such a situation is a function of the application and is not addressed in this manual. The user must refer to appropriate application documentation for applicable procedures for this case. In any event, the safety requirements above must be observed.

3.4.2 Peripheral Hot Swap Procedure

This procedure assumes that the system supports hot swapping, and that the replacement for the board to be hot swapped is configured hardware and software wise for operation in the application.

To hot swap the CP6001 proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

Warning!

Care must be taken when applying the procedures below to ensure that neither the CP6001 nor other system boards are physically damaged by the application of these procedures.

2. Unlock both board ejection handles ensuring that the bottom handle has activated the hot swap switch (this occurs with a very small amount of movement of the handle).

If the blue HS LED is already lit then proceed to step 4, otherwise proceed to step 3.

Note ...

What transpires at this time is a function of the application. If hot swap is supported by the application, then the blue HS LED should light up steady after a short time period or be already lit. This indicates that the system has recognized that the CP6001 is to be hot swapped and now indicates to the operator that hot swapping of the CP6001 may proceed.

If the blue HS LED does not light up after a short time period, either the system does not support hot swap or a malfunction has occurred. In this event, the application is responsible for handling this situation and must provide the operator with appropriate guidance to remedy the situation.

3. After approximately 1 to 15 seconds, the blue HS LED should light up. If the LED lights up, proceed with the next step of this procedure. If the LED does not light up, refer to appropriate application documentation for further action.
4. Disconnect any interfacing cables that may be connected to the board.

Warning!

The CP6001 front panel cables and, when installed, the RIO transition module front panel cables may have power applied which comes from an external source.

In addition, these cables may be connected to devices that can be damaged by electrostatic discharging or short-circuiting of pins.

It is the responsibility of the system designer or integrator to ensure that appropriate measures are taken to preclude damage to the system or injury to personnel which may arise from the handling of these cables (connecting or disconnecting).

Kontron disclaims all liability for damages or injuries resulting from failure to comply with the above.

5. Unscrew the front panel retaining screws.

Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

6. Using the ejector handles, disengage the board from the backplane and carefully remove it from the system.
7. Dispose of the “old” board as required observing the safety requirements indicated in Chapter 3.1.
8. Obtain the replacement CP6001 board.

Warning!

When performing the next step, **DO NOT** push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

9. Carefully insert the “new” board into the “old” board slot until it makes contact with the backplane connectors.
10. Using both ejector handles, engage the board with the backplane. When the ejector handles are locked, the board is engaged.
11. Fasten the front panel retaining screws.
12. Connect all required interfacing cables to the board. Hot swap of the CP6001 is now complete.

Warning!

The CP6001 front panel cables and, when installed, the RIO transition module front panel cables may have power applied which comes from an external source.

In addition, these cables may be connected to devices that can be damaged by electrostatic discharging or short-circuiting of pins.

It is the responsibility of the system designer or integrator to ensure that appropriate measures are taken to preclude damage to the system or injury to personnel which may arise from the handling of these cables (connecting or disconnecting).

Kontron disclaims all liability for damages or injuries resulting from failure to comply with the above.

3.5 Installation of CP6001 Peripheral Devices

The CP6001 is designed to accommodate a variety of peripheral devices whose installation varies considerably. The following chapters provide information regarding installation aspects and not detailed procedures.

3.5.1 USB Device Installation

The CP6001 supports all USB Plug and Play computer peripherals (e.g. keyboard, mouse, printer, etc.).

Note ...

All USB devices may be connected or removed while the host or other peripherals are powered up.

3.5.2 Rear I/O Device Installation

For physical installation of rear I/O devices, refer to the documentation provided with the device itself.

Note ...

COM1 is available at both the CP6001 and the rear I/O transitions module when installed. Use either the front panel or RIO interface, but don’t connect to both at the same time as improper operation will result.

3.5.3 Battery Replacement

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. A suitable battery type is CR2025.

Note ...

The user must be aware that the battery's operational temperature range is less than the storage temperature range of the CP6001.

For exact range information, refer to the battery manufacturer's specifications.

Note ...

Care must be taken to ensure that the battery is correctly replaced.

The battery should be replaced only with an identical or equivalent type recommended by the manufacturer.

Dispose of used batteries according to the manufacturer's instructions.

The typical life expectancy of a 170 mAh battery (CR2025) is 5 - 6 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and the standby time (shutdown time) of the system in which it operates.
To ensure that the lifetime of the battery has not been exceeded it is recommended to exchange the battery after 4 - 5 years.

3.5.4 Hard Disk Installation

The following information pertains to hard disks which may be connected to the CP6001 via normal cabling. SATA devices can be directly connected to the board.

To install a hard disk, it is necessary to perform the following operations in the given order:

1. Install the hardware.

Warning!

The incorrect connection of power or data cables may damage your hard disk unit and/or CP6001 board.

Note ...

Some symptoms of incorrectly installed HDDs are:

- Device on a SATA channel does not spin up: check power cables and cabling. May also result from a bad power supply or SATA drive.
  The SATA connector on the CP6001 provides only a data connection. The power for this device must be supplied by a separate connector. For further information, refer to the respective documentation of the device.
- Hard Disk Drive Fail message at boot-up: may be a bad cable or lack of power going to the drive.

2. Initialize any software necessary to run the chosen operating system.

The following table indicates the ATA channel routing:

Table 3-1: ATA Channel Routing

CHANNEL	DEFAULT
SATA0	Onboard connector J18, for SATA devices (switchable to RIO)
SATA1	Rear I/O module
SATA2	Onboard connector J20, for onboard HDD (switchable to RIO)
SATA3	Rear I/O module

3.6 PMC/CCPMC Module Installation

For the initial installation and standard removal of all PMC or CCPMC modules refer to the documentation provided with the module.

Ensure, however, that prior to installation or removal that the safety requirements indicated in Chapter 3.1 of this User Guide are observed. Particular attention must be paid to the warning regarding the heat sink!

3.7 Software Installation

The installation of all onboard peripheral drivers is described in detail in the relevant Driver Kit files.

Installation of an operating system is a function of the OS software and application requirements, and it is not addressed in this User Guide. Refer to appropriate OS software and application documentation for installation.

Note ...

Users working with pre-configured operating system installation images for Plug and Play compliant operating systems, for example Windows® XP, Windows® XP Embedded, must take into consideration that the stepping and revision ID of the chipset and/or other onboard PCI devices may change. Thus, a re-configuration of the operating system installation image deployed for a previous chipset stepping or revision ID is in most cases required. The corresponding operating system will detect new devices according to the Plug and Play configuration rules.

Installation of application software is not addressed in this User Guide. Refer to appropriate application documentation for installation.

Chapter 4

Configuration

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4. Configuration

4.1 Jumper Description

4.1.1 Clearing BIOS CMOS Setup

If the system does not boot (due to, for example, the wrong BIOS configuration or wrong password setting), the CMOS setting may be cleared by using the solder jumper JP3.

Procedure for clearing CMOS setting:

The system is booted with the jumper in the new, closed position, then powered down again. The jumper is reset back to the normal position, then the system is rebooted again.

Table 4-1: Clearing BIOS CMOS Setup

JP3	DESCRIPTION
Open	***Normal boot using the CMOS settings***
Closed	Clear the CMOS settings and use the default values

The default setting is indicated by using italic bold.

4.1.2 COM2 Termination Jumper Settings

When COM2 is used and is the last device on the RS-422 bus, then the RS-422 interface must provide termination resistance. The purpose of the jumpers JP5 and JP6 is to enable this line termination resistor (120 ohm).

Table 4-2: Jumper Setting for RS-422 TXD Termination (COM2)

JP5	DESCRIPTION
Open	***TXD termination inactive***
Closed	TXD termination active (soldered jumper or 0 ohm resistor in 0805 package)

The default setting is indicated by using italic bold.

Table 4-3: Jumper Setting for RS-422 RXD Termination (COM2)

JP6	DESCRIPTION
Open	***RXD termination inactive***
Closed	RXD termination active (soldered jumper or 0 ohm resistor in 0805 package)

The default setting is indicated by using italic bold.

4.1.3 Shorting Chassis GND (Shield) to Logic GND

The front panel and the front panel connectors are isolated from the logic ground by means of capacitors. If it is necessary to connect the logic GND with the chassis GND, this should be done on the backplane, not on the board itself (see the PICMG CompactPCI Specification 2.0 R3.0, section 3.6).

For further information, refer to the *Kontron* CompactPCI Backplane Manual on the Kontron web site.

4.1.4 BIOS Firmware Hub Flash Configuration

BIOS Firmware Hub Flash configuration means that there are two chips for the BIOS on the CP6001 board. One chip is intended to provide a back-up in the event that the other gets corrupted. If the primary BIOS is corrupted due to physical damage or a faulty Flash upgrade, the 2nd Flash can be selected either via the Board Management Controller or the jumper J16, and the system can boot from it.

Table 4-4: BIOS Firmware Hub Flash Configuration

J16	DESCRIPTION
Open	***Standard FWH is selected***
Closed	Redundant FWH is selected

The default setting is indicated by using italic bold.

4.1.5 M66EN Configuration

The CP6001 can operate at 66 MHz on the CompactPCI interface. If the jumper J17 is set, the frequency is reduced to 33 MHz.

Table 4-5: M66EN Configuration

J17	DESCRIPTION
Open	***PCI speed capability is driven from the backplane***
Closed	PCI 33 MHz

The default setting is indicated by using italic bold.

4.2 Write Protection for Non-Volatile Memory Devices

The CP6001 supports non-volatile memory device write protection via the CompactPCI connector J5, rear I/O signal SYS_WP# (pin E21).

This signal is used to protect all non-volatile memory devices against write and erase cycles. The following table indicates the signal assertion for write protection of the non-volatile memory devices used on the CP6001.

Table 4-6: Write Protection for Non-Volatile Memory Devices

DEVICE	SYS_WP#	
	LOW	HIGH
Redundant FWHs	protected (read-only)	***unprotected (read, write, block erase)***
Serial EEPROM	protected (read-only)	***unprotected (read, write, block erase)***
SPD EEPROM	protected (read-only)	***unprotected (read, write, block erase)***
LAN Configuration EEPROM	protected (read-only)	***unprotected (read, write, block erase)***
Soldered CompactFlash	protected (read-only)	***unprotected (read, write, block erase)***
IPMI Controller (internal Flash)	protected (read-only)	***unprotected (read, write, block erase)***
IPMI Controller (external Flash)	only the top sector is protected (read-only)	***unprotected (read, write, block erase)***
IPMI EEPROM	protected (read-only)	***unprotected (read, write, block erase)***

The default setting is indicated by using italic bold.

Note ...

For normal operation (unprotected), the SYS_WP# signal should be left unconnected. For configurations requiring write protection, this signal must be routed to ground either on the backplane or on the rear I/O module.

4.3 I/O Address Map

The following table indicates the CP6001-specific registers. The blue-shaded table cells indicate BMC-specific registers.

Table 4-7: I/O Address Map

ADDRESS	DEVICE
0x080 - 0x081	BIOS POST Code
0x082 - 0x083	Reserved
0x084 - 0x085	Debug POST Code
0x280	Status Register 0
0x281	Status Register 1
0x282	Control Register 0
0x283	Control Register 1
0x284	Device Protection Register
0x285	Reset Status Register
0x286	Board Interrupt Configuration Register
0x287	Reserved
0x288	Board ID Register
0x289	Board and PLD Revision Register
0x28A	Geographic Addressing Register
0x28B	Delay Timer Register
0x28C	Watchdog Timer Control Register
0x28D - 0x28F	Reserved
0x290	LED Configuration Register
0x291	LED Control Register
0x292	General Purpose Data Register
0x293	General Purpose Control Register
0x294 - 0x299	Reserved
0x29A	IPMI Boot Configuration Register
0x29B	Reserved
0x29C	IPMI Controller Configuration Register
0x29D	IPMI Controller Status Register
0x29E	Reserved
0x29F	IPMI Reset Status Register
0xCA0	IPMI SMM KCS Interface
0xCA1	Reserved
0xCA2 - 0xCA3	IPMI SMS KCS Interface
0xCA4	IPMI SMM KCS Interface

4.4 CP6001-Specific Registers

The following registers are special registers which the CP6001 uses to watch the onboard hardware special features and the CompactPCI control signals.

Normally, only the system BIOS uses these registers, but they are documented here for application use as required.

Note ...
Take care when modifying the contents of these registers as the system BIOS may be relying on the state of the bits under its control.

4.4.1 Status Register 0

The Status Register 0 holds general/common status information.

Table 4-8: Status Register 0

REGISTER NAME		STATUS REGISTER 0		
ADDRESS		0x280		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	HSHS	Hot swap handle status: 0 = Hot swap handle in closed position 1 = Hot swap handle in open position	N/A	R
6	BBEI	BIOS boot end indication: 0 = BIOS is booting 1 = BIOS boot is finished	0	R
5 - 4	BFSS	Boot Flash selection status: 00 = Boot Flash 0 active 01 = Boot Flash 1 active 10 = External boot Flash active	N/A	R
3 - 0	Res.	Reserved	0000	R

4.4.2 Status Register 1

The Status Register 1 holds board-specific status information.

Table 4-9: Status Register 1

REGISTER NAME		STATUS REGISTER 1		
ADDRESS		0x281		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	C66EN	CPCI PCI speed (M66EN signal): 0 = 33 MHz 1 = 66 MHz	N/A	R
6	CXCAP	CPCI PCI bus protocol (PCIXCAP signal): 0 = Standard PCI protocol 1 = PCI-X protocol	N/A	R
5	P66EN	PMC PCI speed (M66EN signal): 0 = 33 MHz 1 = 66 MHz	N/A	R
4	PXCAP	PMC PCI bus protocol (PCIXCAP signal): 0 = Standard PCI protocol 1 = PCI-X protocol	N/A	R
3	CSYS	CPCI system slot identification (SYSEN signal): 0 = Installed in a system slot 1 = Installed in a peripheral slot	N/A	R
2	CENUM	CPCI system enumeration (ENUM signal): 0 = Indicates the insertion or removal of a hot swap system board 1 = No hot swap event	N/A	R
1	CFAL	CPCI power supply status (FAL signal): 0 = Power supply failure 1 = Power in normal state	N/A	R
0	CDEG	CPCI power supply status (DEG signal): 0 = Power derating 1 = Power in normal state	N/A	R

4.4.3 Control Register 0

The Control Register 0 holds one bit for specifying the boot Flash to be updated.

Table 4-10: Control Register 0

REGISTER NAME		CONTROL REGISTER 0		
ADDRESS		0x282		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 6	Res.	Reserved	00	R
5	BFUS	Boot Flash update selection: 0 = Select default boot Flash for update 1 = Select alternative boot Flash for update	0	R/W
4 - 0	Res.	Reserved	00000	R

4.4.4 Control Register 1

The Control Register 1 holds board-specific control information.

Table 4-11: Control Register 1

REGISTER NAME		CONTROL REGISTER 1		
ADDRESS		0x283		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 6	Res.	Reserved	00	R
5	TPMR	Trusted Platform Module (TPM) reset: 0 = Disable TPM reset 1 = Enable TPM reset	0	R/W
4	CRST	CPCI reset in peripheral slot: 0 = Disable CPCI reset to board 1 = Enable CPCI reset to board	0	R/W
3 - 2	Res.	Reserved	00	R
1	ECFG1	Ethernet I/O configuration GbE B: 0 = Front I/O 1 = Rear I/O	0	R/W
0	ECFG0	Ethernet I/O configuration GbE A: 0 = Front I/O 1 = Rear I/O	0	R/W

4.4.5 Device Protection Register

The Device Protection Register holds the write protect signals for Flash devices.

Table 4-12: Device Protection Register

REGISTER NAME		DEVICE PROTECTION REGISTER		
ADDRESS		0x284		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	SWP	System Write Protection 0 = Non-volatile memory not write protected 1 = Non-volatile memory write protected	0	R
6 - 3	Res.	Reserved	0000	R
2	IFWP	IDE Flash write protection: 0 = IDE Flash not write protected 1 = IDE Flash write protected Writing a '1' to this bit sets the bit. If the bit is set, it cannot be cleared.	0	R/W
1	Res.	Reserved	0	R
0	BFWP	Boot Flash write protection: 0 = Boot Flash not write protected 1 = Boot Flash write protected Writing a '1' to this bit sets the bit. If the bit is set, it cannot be cleared. This bit protects both Boot Flashes.	0	R/W

4.4.6 Reset Status Register

The Reset Status Register is used to determine the host's reset source.

Table 4-13: Reset Status Register

REGISTER NAME		RESET STATUS REGISTER		
ADDRESS		0x285		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	PORS	Power-on reset status: 0 = System reset generated by software (warm reset) 1 = System reset generated by power-on (cold reset) Writing a '1' to this bit clears the bit.	N/A	R/W
6	Res.	Reserved	0	R
5	SRST	Software reset status: 0 = Reset is logged by BMC 1 = Reset is not logged by BMC The BIOS/software sets the bit to inform the BMC that the next reset should not be logged. Writing a '1' from the host to this bit sets the bit. After setting the bit, it may be cleared via the BMC (using the IPMI Reset Status Register and an I²C access from the BMC to this register by writing a '1' to the SRST bit).	0	R/W
4	Res.	Reserved	0	R
3	IPRS	IPMI controller reset: 0 = System reset not generated by IPMI 1 = System reset generated by IPMI Writing a '1' to this bit clears the bit.	0	R/W
2	FPRS	Front panel push button reset status: 0 = System reset not generated by front panel reset 1 = System reset generated by front panel reset Writing a '1' to this bit clears the bit.	0	R/W
1	CPRS	CompactPCI reset status (PRST signal): 0 = System reset not generated by CPCI reset input 1 = System reset generated by CPCI reset input Writing a '1' to this bit clears the bit.	0	R/W
0	WTRS	Watchdog timer reset status: 0 = System reset not generated by Watchdog timer 1 = System reset generated by Watchdog timer Writing a '1' to this bit clears the bit.	0	R/W

Note ...

The reset status register is set to the default values by power-on reset, not by PCI reset.

4.4.7 Board Interrupt Configuration Register

Table 4-14: Board Interrupt Configuration Register

REGISTER NAME		BOARD INTERRUPT CONFIGURATION REGISTER		
ADDRESS		0x286		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 6	CFICF	CPCI fail signal interrupt configuration (FAL signal): 00 = Disabled 01 = IRQ5 10 = Reserved 11 = Reserved	00	R
5	CEICF	CPCI enumeration signal to IRQ5 routing (ENUM signal): 0 = Disabled 1 = Enabled	0	R/W
4	CDICF	CPCI derate signal to IRQ5 routing (DEG signal): 0 = Disabled 1 = Enabled	0	R/W
3 - 2	Res.	Reserved	00	R
1 - 0	WICF	Watchdog interrupt configuration: 00 = Disabled 01 = IRQ5 10 = Reserved 11 = Reserved	00	R/W

4.4.8 Board ID Register

Each Kontron board is provided with a unique board-type identifier in the form of a hexadecimal number, as indicated in the following register.

Table 4-15: Board ID Register

REGISTER NAME		BOARD ID REGISTER		
ADDRESS		0x288		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 0	BID	Board identification: 0xAA = CP6001	0xAA	R

4.4.9 Board and PLD Revision Register

This register reflects the current revision status for the board's hardware and the logic contained in the Programmable Logic Device (PLD). Application software can use this information to identify possible functional differences which require handling by the software. The initial setting for the CP6001 is 0x80.

Table 4-16: Board and PLD Revision Register

REGISTER NAME		BOARD AND PLD REVISION REGISTER		
ADDRESS		0x289		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 4	BREV	Board revision	N/A	R
3 - 0	PREV	PLD revision	N/A	R

4.4.10 Geographic Addressing Register

Table 4-17: Geographic Addressing Register

REGISTER NAME		GEOGRAPHIC ADDRESSING REGISTER		
ADDRESS		0x28A		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 5	Res.	Reserved	000	R
4 - 0	GA	CPCI geographic address	N/A	R

Note ...

The Geographic Addressing Register is set to the default values by power-on reset, not by PCI reset.

4.4.11 Delay Timer Register

The delay timer enables the user to realize short, reliable delay times. It runs by default and does not start again on its own. It can be restarted at anytime by writing anything other than a ’0’ to the Delay Timer Register. The hardware delay timer provides a set of outputs for defined elapsed time periods. The timer outputs reflected in the Delay Timer Register are set consecutively and remain set until the next restart is triggered again.

Table 4-18: Delay Timer Register

REGISTER NAME		DELAY TIMER REGISTER		
ADDRESS		0x28B		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 0	DTC	The hardware delay timer is operated via one simple 8-bit control/ status register. During normal operation, each of the 8 bits reflects a timer output which means defined elapsed time period after the last restart according to the following bit mapping: **DTC[7:0] Value Accuracy** Bit 7: 1 ms < + 0.04% Bit 6: 500 µs < + 0.08% Bit 5: 250 µs < + 0.16% Bit 4: 100 µs < + 0.4% Bit 3: 50 µs < + 0.8% Bit 2: 10 µs < + 4% Bit 1: 5 µs < + 8% Bit 0: 1 µs < + 40%	0x00	R/W

Since the timer width and thus the availability of outputs varies over different implementations, it is necessary to be able to determine the timer capability. Therefore, writing a ’0’ to the Delay Timer Register followed by reading indicates the timer capability (not the timer outputs). For example, writing 0x00 and then reading 0xFF results in a 8-bit wide timer register. This status register mode can be switched off to normal timer operation by writing anything other than a ’0’ to this register.

4.4.12 Watchdog Timer Control Register

The CP6001 has one Watchdog Timer provided with a programmable timeout ranging from 125 msec to 256 sec. Failure to strobe the Watchdog Timer within a set time period results in a system reset or an interrupt. The interrupt mode can be configured via the Board Interrupt Configuration Register (0x286).

There are four possible modes of operation involving the Watchdog Timer:

- Timer only mode
- Reset mode
- Interrupt mode
- Dual stage mode

At power on the Watchdog is not enabled. If not required, it is not necessary to enable it. If required, the bits of the Watchdog Timer Control Register (0x282) must be set according to the application requirements. To operate the Watchdog, the mode and time period required must first be set and then the Watchdog enabled. Once the Watchdog is enabled, it is not possible to change either the mode, the timeout period, or to disable the Watchdog as long as power is applied to the system. To prevent a Watchdog timeout, the Watchdog must be retriggered before timing out. This is done by writing a ’1’ to the WTR bit. In the event a Watchdog timeout does occur, the WTE bit is set to ’1’. What transpires after this depends on the mode selected.

The four operational Watchdog Timer modes can be configured by the WMD[1:0] bits, and are described as follows:

Timer only mode - In this mode the Watchdog is enabled using the required timeout period. Normally, the Watchdog is retriggered by writing a ’1’ to the WTR bit. In the event a timeout occurs, the WTE bit is set to ’1’. This bit can then be polled by the application and handled accordingly. To continue using the Watchdog, write a ’1’ to the WTE bit, and then retrigger the Watchdog using WTR. The WTE bit retains its setting as long as no power down-up is done. Therefore, this bit may be used to verify the status of the Watchdog.

Reset mode - This mode is used to force a hard reset in the event of a Watchdog timeout. In addition, the WTE bit is not reset by the hard reset, which makes it available if necessary to determine the status of the Watchdog prior to the reset.

Interrupt mode - This mode causes the generation of an interrupt in the event of a Watchdog timeout. The interrupt handling is a function of the application. If required, the WTE bit can be used to determine if a Watchdog timeout has occurred.

Dual stage mode - This is a complex mode where in the event of a timeout two things occur: 1) an interrupt is generated, and 2) the Watchdog is retriggered automatically. In the event a second timeout occurs immediately following the first timeout, a hard reset will be generated. If the Watchdog is retriggered normally, operation continues. The interrupt generated at the first timeout is available to the application to handle the first timeout if required. As with all of the other modes, the WTE bit is available for application use.

Table 4-19: Watchdog Timer Control Register

REGISTER NAME		WATCHDOG TIMER CONTROL REGISTER		
ADDRESS		0x28C		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	WTE	Watchdog Timer expired status bit: 0 = Watchdog Timer has not expired 1 = Watchdog Timer has expired. Writing a '1' to this bit resets it to 0.	0	R/W
6 - 5	WMD	Watchdog Mode: 00 = Timer only mode 01 = Reset mode 10 = Interrupt mode 11 = Cascaded mode (dual-stage mode)	00	R/W
4	WEN/WTR	Watchdog enable / Watchdog trigger control bit: 0 = Watchdog Timer not enabled Prior to the Watchdog being enabled, this bit is known as WEN. After the Watchdog is enabled, it is known as WTR. Once the Watchdog Timer has been enabled, this bit cannot be reset to 0. As long as the Watchdog Timer is enabled, it will indicate a '1'. 1 = Watchdog Timer enabled Writing a '1' to this bit causes the Watchdog to be retriggered to the timer value indicated by bits WTM[3:0].	0	R/W
3 - 0	WTM	Watchdog timeout settings: 0000 = 0.125 s 0001 = 0.25 s 0010 = 0.5 s 0011 = 1 s 0100 = 2 s 0101 = 4 s 0110 = 8 s 0111 = 16 s 1000 = 32 s 1001 = 64 s 1010 = 128 s 1011 = 256 s 1100 = reserved 1101 = reserved 1110 = reserved 1111 = reserved The nominal timeout period is 5% longer than the above-stated values.	0000	R/W

4.4.13 LED Configuration Register

The LED Configuration Register holds a series of bits defining the onboard configuration for the front panel LEDs.

Table 4-20: LED Configuration Register

REGISTER NAME		LED CONFIGURATION REGISTER		
ADDRESS		0x290		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 4	Res.	Reserved	0000	R
3 - 0	LCON	General Purpose LED Configuration: 0000 = POST [1)] 0001 = General Purpose Mode[2)] 0010 - 1111 = Reserved	0000	R/W

Regardless of the selected configuration, the General Purpose LEDs are used to signal a number of fatal onboard hardware errors, such as:

LED3: BIOS boot fail (red)
LED2: BIOS boot fail (red)
LED1: Hardware reset (red)
LED0: Power-on reset (red)

[1)] In BIOS POST mode (default), the LEDs build a binary vector to display BIOS POST code during the BIOS boot phase. In doing so, the higher 4-bit nibble of the 8-bit BIOS POST code is displayed followed by the lower nibble followed by a pause. BIOS POST code is displayed in general in green color.

LED3: POST bit 3 and bit 7 (green)
LED2: POST bit 2 and bit 6 (green)
LED1: POST bit 1 and bit 5 (green)
LED0: POST bit 0 and bit 4 (green)

For further information on reading the 8-bit BIOS POST Code, refer to Chapter 2.3.1.3, “General Purpose LEDs”.

[2)] Configured for General Purpose Mode, the LEDs are dedicated to functions as follows:

LED3: LED 3, controlled by HOST (red/green)
LED2: LED 2, controlled by HOST (red/green)
LED1: LED 1, controlled by HOST (red/green)
LED0: LED 0, controlled by HOST (red/green)

4.4.14 LED Control Register

The LED Control Register enables the user to switch on and off the General Purpose LEDs.

Table 4-21: LED Control Register

REGISTER NAME		LED CONTROL REGISTER		
ADDRESS		0x291		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 4	LCMD	LED command: 0000 = Get LED 0 0001 = Get LED 1 0010 = Get LED 2 0011 = Get LED 3 0100 - 0111 = Reserved 1000 = Set LED 0 1001 = Set LED 1 1010 = Set LED 2 1011 = Set LED 3 1100 - 1111 = Reserved	0	R/W
3 - 0	LCOL	LED color: 0000 = Off 0001 = Green 0010 = Red 0011 = Amber 0100 - 1111 = Reserved	0000	R/W

Note ...

This register can only be used if the General Purpose LEDs indicated in the “LED Configuration Register” (Table 4-20) are configured in General Purpose Mode.

4.4.15 General Purpose Data Register

This register is used in conjunction with the General Purpose Control Register to control the functionality of the signals GPIO0 (pin A20) and GPIO1 (pin D20) on the J5 rear I/O connector.

Table 4-22: General Purpose Data Register

REGISTER NAME		GENERAL PURPOSE DATA REGISTER		
ADDRESS		0x292		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 2	Res.	Reserved	000000	R
1	GPIO1	GPIO data Output: 0 = GPIO1 is driven low 1 = GPIO1 is driven high Input: 0 = GPIO1 is externally driven low 1 = GPIO1 is externally driven high	0	R/W
0	GPIO0	GPIO data Output: 0 = GPIO0 is driven low 1 = GPIO0 is driven high Input: 0 = GPIO0 is externally driven low 1 = GPIO0 is externally driven high	0	R/W

4.4.16 General Purpose Control Register

This register is used in conjunction with the General Purpose Data Register to control the functionality of the signals GPIO0 (pin A20) and GPIO1 (pin D20) on the J5 rear I/O connector.

Table 4-23: General Purpose Control Register

REGISTER NAME		GENERAL PURPOSE CONTROL REGISTER		
ADDRESS		0x293		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 2	Res.	Reserved	000000	R
1	GPIO1	GPIO1 control: 0 = GPIO1 is input 1 = GPIO1 is output	0	R/W
0	GPIO0	GPIO0 control: 0 = GPIO0 is input 1 = GPIO0 is output	0	R/W

4.5 BMC-Specific Registers

The following registers are special registers which the CP6001 uses to monitor and configure the Board Management Controller.

4.5.1 IPMI Boot Configuration Register

With the IPMI Boot Configuration Register the IPMI can configure a number of BIOS settings. This register is read only from the host side and will be configured only by the Board Management Controller (BMC).

Table 4-24: IPMI Boot Configuration Register

REGISTER NAME		IPMI BOOT CONFIGURATION REGISTER		
ADDRESS		0x29A		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 3	Res.	Reserved	00000	R
2 - 0	BOCON	BIOS boot order configuration: 000 = Boot order is according to BIOS setup (default) 001 = Next boot device class: FDD 010 = Next boot device class: HDD 011 = Next boot device class: CD-ROM 100 = Next boot device class: Network 101 = Next boot device class: USB FDD 110 = Next boot device class: USB HDD 111 = Next boot device class: USB CD-ROM	000	R

Note ...

This register is set to the default values by power-on reset, not by PCI reset. The BIOS boot order can also be configured in the BIOS.

4.5.2 IPMI Controller Configuration Register

Table 4-25: IPMI Controller Configuration Register

REGISTER NAME		IPMI CONTROLLER CONFIGURATION REGISTER		
ADDRESS		0x29C		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	IPGC	IPMI program request: 0 = No action 1 = Request IPMI to program the internal Flash from the external Flash	0	R/W
6	IPGU	IPMI enforces the User Program Mode / Mode 2: 0 = No action 1 = Set IPMI in User Program Mode / Mode 2 This bit is ignored if IPMI is in local programming mode.	0	R/W
5 - 4	Res.	Reserved	00	R
3	ICOMT	IPMI serial port configuration for debugging: 0 = IPMI serial port is connected to the COM front panel RJ-45 connector (only for debugging purposes) 1 = IPMI serial port is isolated	1	R
2	ISCI	IPMI serial port configuration for firmware update: 0 = IPMI serial port disabled 1 = IPMI serial port is connected to the host port COM2	0	R/W
1	IRST	IPMI reset function: 0 = IPMI controller is running 1 = IPMI controller is in reset state	0	R/W
0	IPGM	IPMI program mode for selecting the firmware update mode: 0 = Normal operating mode 1 = Set IPMI in firmware update mode	0	R/W

The following table indicates the COM port routing for the firmware update and debugging purposes.

Table 4-26: COM Port Routing for the Firmware Update and Debugging Purposes

IPGM	ISCI	ICOMT	IPMI SERIAL PORT	SUPER I/O COM2 PORT
0	0	1	Disabled	Connected to rear I/O
0	1	1	Connected to Super I/O COM2 port	Connected to IPMI serial port
0	--	0	Connected to the COM1 front panel RJ-45 connector	Connected to rear I/O
1	--	--	Connected to Super I/O COM2 port	Connected to IPMI serial port

Note ...

To allow updating the firmware of the Module Management Controller, the software must set IRST and IPGM, and clear IRST after 20 ms. Now, IPMI boots from the COM2 port. After programming is completed, IRST must be set and IPGM must be cleared. After 20 ms, IRST must be cleared again. IPMI now boots from its own internal flash.

Note ...

For debugging purposes, the IPMI serial port can be switched via the PLD to the COM connector, J12. In this configuration, both serial ports COM1 (RX/TX) and the IPMI serial port (RX/TX) are routed to J12. For further information on the IPMI signals on the COM1 port, refer to Chapter 2.3.4, COM Ports, Table 2-14.

4.5.3 IPMI Controller Status Register

Table 4-27: IPMI Controller Status Register

REGISTER NAME		IPMI CONTROLLER STATUS REGISTER		
ADDRESS		0x29D		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	IFSEL	IPMI Firmware hub selection: 0 = Select the second FWH boot device 1 = Default FWH boot device is active	1	R
6 - 3	Res.	Reserved	1111111	R

Note ...

This register can be configured only by the IPMI controller and is set to the default values by power-on reset, not by PCI reset.

4.5.4 IPMI Reset Status Register

The IPMI Reset Status Register is used to determine the IPMI reset source.

Table 4-28: IPMI Reset Status Register

REGISTER NAME		IPMI RESET STATUS REGISTER		
ADDRESS		0x29F		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	PORS	Power-on reset detection (IPMI side): 0 = System reset generated by software (warm reset) 1 = System reset generated by power-on (cold reset) This bit may be cleared only by IPMI. Writing a '1' from IPMI to this bit cleares the bit.	N/A	R
6	Res.	Reserved	0	R
5	SRST	Software reset status: 0 = Reset is logged by IPMI 1 = Reset is not logged by IPMI The BIOS/software sets this bit to inform the BMC that the next reset will not be logged. The bit can only be set from the host side through the use of the Reset Status Register register (by writing there a '1' to the SRST bit.) Writing a '1' from IPMI to this bit cleares the bit.	0	R
4	Res.	Reserved	0	R
3	IPRS	IPMI controller reset: 0 = System reset not generated by IPMI 1 = System reset generated by IPMI Writing a '1' from IPMI to this bit cleares the bit.	0	R
2	FPRS	Front panel bush button reset status: 0 = System reset not generated by front panel reset 1 = System reset generated by front panel reset Writing a '1' from IPMI to this bit cleares the bit.	0	R/W
1	CPRS	CompactPCI reset status: 0 = System reset not generated by CPCI reset input 1 = System reset generated by CPCI reset input Writing a '1' from IPMI to this bit cleares the bit.	0	R/W
0	WTRS	Watchdog timer reset status: 0 = System reset not generated by Watchdog timer 1 = System reset generated by Watchdog timer Writing a '1' from IPMI to this bit cleares the bit.	0	R/W

Note ...

This register is set to the default values by power-on reset, not by PCI reset.

4.5.5 IPMI Keyboard Control Style Interface

The host processor communicates with the BMC using two Keyboard Control Style (KCS) interfaces, which are defined in the IPMI specification. One interface is for the System Management Software (SMS) used within an operating system, and one for the System Management Mode (SMM) used only by the BIOS.

The KCS interface for the system management software is on the I/O location 0xCA2 and 0xCA3, and configured as regular ISA interrupt.

The KCS interface for the system management mode is on the I/O location 0xCA0 and 0XCA4, and configured as SMI interrupt.

Chapter 5

Power Considerations

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5. Power Considerations

5.1 System Power

The considerations presented in the ensuing chapters must be taken into account by system integrators when specifying the CP6001 system environment.

5.1.1 CP6001 Baseboard

The CP6001 baseboard itself has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the CP6001 should be carefully tested to ensure compliance with these ratings.

Table 5-1: Maximum Input Power Voltage Limits

SUPPLY VOLTAGE	MAXIMUM PERMITTED VOLTAGE
+3.3 V	+3.6 V
+5 V	+5.5 V
+12 V	+14.0 V
-12 V	-14.0 V

Warning!

The maximum permitted voltage indicated in the table above must not be exceeded. Failure to comply with the above may result in damage to your board.

The following table specifies the ranges for the different input power voltages within which the board is functional. The CP6001 is not guaranteed to function if the board is not operated within the prescribed limits.

Table 5-2: DC Operational Input Voltage Ranges

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE	RECOMMENDED RANGE
+3.3 V	3.2 V min. to 3.47 V max.	3.3 V min. to 3.47 V max.
+5 V	4.85 V min. to 5.25 V max.	5.0 V min. to 5.25 V max.
+12 V	11.4 V min. to 12.6 V max.	12 V min. to 12.6 V max.
-12 V	-11.4 V min. to -12.6 V max.	Only for PMC/CCPMC

5.1.2 Backplane

Backplanes to be used with the CP6001 must be adequately specified. The backplane must provide optimal power distribution for the +3.3 V, +5 V and +12 V power inputs.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under-dimensioned cabling or bridges, high-resistance connections, etc. must be avoided. It is recommended to use POSITRONIC or M-type connector backplanes and power supplies where possible.

5.1.3 Power Supply Units

Power supplies for the CP6001 must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. An industrial power supply unit should be able to provide at least twice as much power as the entire system requires. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

As the design of the CP6001 has been optimized for minimal power consumption, the power supply unit shall be stable even without minimum load.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for backplane input line resistance variations due to temperature changes, etc.

Note ...

Non-industrial ATX PSUs may require a greater minimum load than a single CP6001 is capable of creating. When a PSU of this type is used, it may not power up correctly and cause the CP6001 to hang up. The solution is to use an industrial PSU or to add more load to the system.

5.1.3.1 Start-Up Requirement

Power supplies must comply with the following guidelines, in order to be used with the CP6001.

- Beginning at 10% of the nominal output voltage, the voltage must rise within > 0.1 ms to < 20 ms to the specified regulation range of the voltage. Typically: > 5 ms to < 15 ms.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band.
- The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0 V to nominal Vout.

Warning!

For BIOS initialization of certain interfaces, the 3.3 V input power supply must be able to provide a minimum peak current of 10 A to the CP6001. This applies for each CP6001 in a given system.

Failure to comply with the above warning may result in improper operation of the CP6001.

5.1.3.2 Power-Up Sequence

The +5 VDC output level must always be equal to or higher than the +3.3 VDC output during power-up and normal operation. Both voltages must reach their minimum in-regulation level not later than 20 ms after the output power ramp start.

5.1.3.3 Tolerance

The tolerance of the voltage lines is described in the CPCI specification (PICMG 2.0 R3.0).The recommended measurement point for the voltage is the CPCI connector on the CPU board.

The following table provides information regarding the required characteristics for each board input voltage.

Table 5-3: Input Voltage Characteristics

VOLTAGE	NOMINAL VALUE	TOLERANCE	MAX. RIPPLE (p-p)	REMARKS
5 V	+5.0 VDC	+5%/-3%	50 mV	Main voltage
3.3 V	+3.3 VDC	+5%/-3%	50 mV	--
+12 V	+12 VDC	+5%/-5%	240 mV	Required
-12 V	-12 VDC	+5%/-5%	240 mV	Not required
VI/O (PCI) voltage	+3.3 VDC or +5 VDC	+5%/-3%	50 mV	--
GND	Ground, not directly connected to potential earth (PE)			

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

5.1.3.4 Regulation

The power supply shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

Warning!

All of the input voltages must be functionally coupled to each other so that if one input voltage fails, all other input voltages must be regulated proportionately to the failed voltage. For example, if the +5V begins to decrease, all other input voltages must decrease accordingly. This is required in order to preclude cross currents within the CP6001.

Failure to comply with above may result in damage to the board or improper system operation.

Note ...

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until capacitors are discharged. If the voltage rises again before it has gone below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 30 seconds before it may be switched on again. If short interruptions of the power supply still occur, it is recommended to use uninterrupted power supply units or power-on delay devices.

5.2 Power Consumption

The goal of this description is to provide a method to calculate the power consumption for the CP6001 baseboard and for additional configurations. The processor dissipates the majority of the thermal power.

The power consumption tables below list the voltage and the power specifications for the CP6001 board and its accessories. The values were measured using an 8-slot passive CompactPCI backplane with two power supply units, one for the CPU, and the other for the hard disk. The operating systems used were DOS, Linux and Windows® XP. All measurements were conducted at a temperature of 25°C. The measured values varied, because the power consumption was dependent on the processor activity.

Note ...

The power consumption values indicated in the tables below can vary depending on the ambient temperature or the system performance. This can result in deviations of the power consumption values of up to 10%.

The power consumption was measured using the following processors:

- Intel® Core™ Duo, U2500 (ULV), 1.2 GHz, 533 MHz FSB, 2 MB L2 cache
- Intel® Core™2 Duo, L7400 (LV), 1.5 GHz, 667 MHz FSB, 4 MB L2 cache

with the following operating systems:

- DOS
  With this operating system only one processor core was active. This operating system has no power management support and provides a very simple method to verify the measured power consumption values.
- Linux/Windows® XP, IDLE Mode
  With these operating systems both processor cores were in IDLE state.

and under the following testing conditions:

- CP6001 Thermal Design Power (TDP) at 75%
  These values represent the “typical” maximum power dissipation reached under OS-controlled applications.
- CP6001 Thermal Design Power (TDP) at 100%
  These values represent the maximum power dissipation achieved through the use of specific tools to heat up the processor cores. 100% TDP is unlikely to be reached in real applications.

The following tables indicate the power consumption of the CP6001 with 1 GB DDR2 SDRAM in dual-channel mode. For measurements made with the Linux and Windows® XP operating systems, the VGA resolution was 1280 x 1024 pixels.

Table 5-4: Power Consumption: CP6001 with DOS

POWER	CORE™ DUO 1.2 GHz (ULV) 2 MB	Core™2 DUO 1.5 GHz (LV) 4 MB
12 V	50 mW	50 mW
5 V	6 W	9 W
3.3 V	10 W	10 W
Total	16 W	19 W

Table 5-5: Power Consumption: CP6001 with Linux/Win. XP in IDLE Mode

POWER	CORE™ DUO 1.2 GHz (ULV) 2 MB	Core™2 DUO 1.5 GHz (LV) 4 MB
12 V	50 mW	50 mW
5 V	3 W	5 W
3.3 V	10 W	10 W
Total	13 W	15 W

Table 5-6: Power Consumption: CP6001 at 75% TDP

POWER	CORE™ DUO 1.2 GHz (ULV) 2 MB	Core™2 DUO 1.5 GHz (LV) 4 MB
12 V	50 mW	50 mW
5 V	7 W	14 W
3.3 V	10 W	10 W
Total	17 W	24 W

Table 5-7: Power Consumption: CP6001 at 100% TDP

POWER	CORE™ DUO 1.2 GHz (ULV) 2 MB	Core™2 DUO 1.5 GHz (LV) 4 MB
12 V	50 mW	50 mW
5 V	9 W	17 W
3.3 V	10 W	10 W
Total	19 W	27 W

5.2.1 Power Consumption of the CP6001 Accessories

The following table indicates the power consumption of the CP6001 accessories.

Table 5-8: Power Consumption of CP6001 Accessories

MODULE	POWER 5 V	POWER 3.3 V AVERAGE
Keyboard	100 mW	—
DDR2 SDRAM update from 1 GB to 2 GB	—	approx. 4 W
DDR2 SDRAM update from 2 GB to 4 GB	—	approx. 6 W
USB NAND Flash module	325 mW - 400 mW	—

5.2.2 Power Consumption of the Gigabit Ethernet Controller

The following table indicates the additional power consumption of the Intel® 82573L Gigabit Ethernet controller.

Table 5-9: Intel® 82573L Gigabit Ethernet Controller Power Consumption

ETHERNET PORT	SPEED	POWER
One Ethernet port plugged	100 Mb/s	0.33 W
One Ethernet port plugged	1000 Mb/s	1.21 W

5.3 Start-Up Currents of the CP6001

The following table indicates the basic start-up currents of the CP6001 during the first 2-3 seconds after power has been applied (power-on or hot-swap insertion). In addition to these values, each time when the BIOS initializes the interfaces (power-on, hot swap, reset), there can be a peak load of 10 A on the 3.3 V input power supply.

Table 5-10: Start-Up Currents of the CP6001

POWER		CORE™ DUO 1.2 GHz (ULV) 1 GB sold. DDR2	Core™2 DUO 1.5 GHz (LV) 1 GB sold. DDR2
5 V	peak	6.9 A	6.9 A
	average	2.0 A	2.0 A
3.3 V	peak	5.1 A	5.1 A
	average	3.2 A	3.2 A

For further information on the start-up current, please contact Kontron.

Warning!

For BIOS initialization of certain interfaces, the 3.3 V input power supply must be able to provide a minimum peak current of 10 A to the CP6001. This applies for each CP6001 in a given system.

Failure to comply with the above warning may result in improper operation of the CP6001.

5.4 Power Available for PMC Devices

The following table indicates the power made available by the CP6001 to PMC devices.

Table 5-11: Maximum Output Power Limits

VOLTAGE	CONTINUOUS CURRENT	PEAK CURRENT
+3.3 V	2.27 A	4.0 A
+5 V	1.5 A	3.0 A*
+12 V	0.6 A	0.8 A
-12 V	0.4 A	0.4 A

* The maximum current available on the PMC module varies depending on the CPU load.

Note ...

A maximum power of 7.5 W is available on the pins of the PMC connectors Jn1 and Jn2 which provide a voltage of 3.3 V or 5 V. This is in accordance with the draft standard P1386/Draft 2.4a. The maximum power of 7.5 W can be arbitrarily divided on the 3.3 V and 5 V voltage lines.

The +12 V and -12 V voltage lines are only required for operation of PMC modules. Their availability depends on the power supply.

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Chapter 6

Thermal Considerations

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6. Thermal Considerations

The following chapters provide system integrators with the necessary information to satisfy thermal and airflow requirements when implementing CP6001 applications.

6.1 Board Internal Thermal Monitoring

To ensure optimal operation and long-term reliability of the CP6001, all onboard components must remain within the maximum temperature specifications. The most critical components on the CP6001 are the processor and the chipset. Operating the CP6001 above the maximum operating limits will result in permanent damage to the board. To ensure functionality at the maximum temperature, the BIOS and the Board Management Controller support several temperature monitoring and control features.

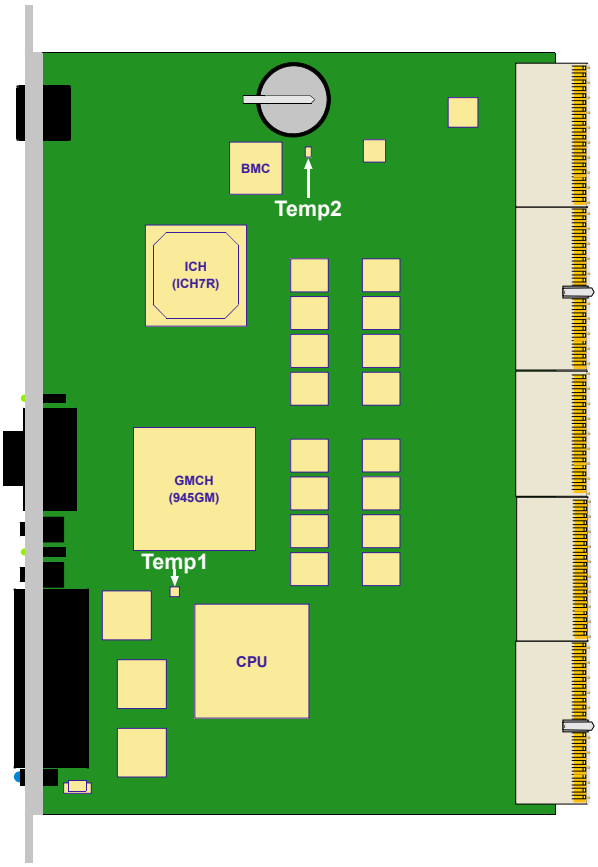
The CP6001 includes four temperature sensors distributed over the complete board to measure the onboard temperature values and regulate the board's power consumption:

- Thermal sensors integrated in the processor
- Onboard temperature sensor Temp1 (near the BMC)
- Onboard temperature sensor Temp2 (between the CPU and the chipset)
- Temperature sensor integrated in the Super I/O (see Figure 1-5)

The onboard temperature sensors Temp1 and Temp2 are accessible via the Board Management Controller. The temperature sensor integrated on the Super I/O is accessible via the host. For information on the temperature sensors integrated in the CPU, refer to Chapter 6.2.

6.1.1 Placement of the Temperature Sensors

Figure 6-1: Temperature Sensor Placement (CP6001 Top View)



6.2 Processor Thermal Monitoring and Regulation

The Intel® Core™ Duo / Core™2 Duo processor includes the following on-die temperature sensors:

- Two Digital Thermal Sensors (DTS)
- Thermal Diode Sensor
- Thermal Monitor 1 (TM1) Sensor
- Thermal Monitor 2 (TM2) Sensor
- Catastrophic Cooling Failure Sensor

Via the Thermal Diode Sensor, the Board Management Controller can measure the processor die temperature. Via the Digital Thermal Sensor (DTS), the BIOS or the application software can measure the processor die temperature.

The Thermal Monitor 1 (TM1) Sensor, the Thermal Monitor 2 (TM2) Sensor, and the Catastrophic Cooling Failure Sensor are not accessible. They serve for protecting the processor from overheating. These sensors are integrated in the processor and work without any interoperability of the Board Management Controller, the BIOS or the software application. The thermal monitor function utilizes the thermal control circuit to regulate the processor temperature. It is enabled in the BIOS and allows the processor to maintain a safe operating temperature without the need for special software drivers or interrupt handling routines.

The maximum die temperatures for all processor types is as follows:

- Intel® Core™ Duo: all versions: 100°C
- Intel® Core™2 Duo: all versions: 100°C

6.2.1 Digital Thermal Sensor (DTS)

The processor includes two on-die Digital Thermal Sensors (DTS) that can be read via an internal register of the processor (no I/O interface). The Digital Thermal Sensors provide the preferred method of reading the processor die temperature since they are located much closer to the hottest portions of the die and can thus more accurately track the die temperature.

The values measured at the Digital Thermal Sensors (DTS) may not correspond to the values measured at the Thermal Diode Sensor since the Thermal Diode Sensor is located elsewhere on processor die.

6.2.2 Thermal Diode Sensor

The processor includes one Thermal Diode Sensor used by the Board Management Controller to measure the processor die temperature.

6.2.3 Thermal Monitor 1 (TM1)

The Thermal Monitor 1 (TM1) Sensor controls the processor temperature and power consumption by activating the Thermal Control Circuit (TCC) when the processor silicon reaches its maximum operating temperature (100°C).

When TM1 is enabled and a high temperature situation exists, the processor clock is modulated using duty cycles and reports to the BMC a throttle event, which is reflected in the CPU0 status sensors. Once the temperature has dropped below the maximum operating temperature, the Thermal Control Circuit goes inactive.

The temperature at which TM1 activates the Thermal Control Circuit is neither user-configurable nor software-visible.

TM1 does not require any additional hardware, software drivers, or interrupt handling routines. This function can be enabled and disabled in the BIOS.

Note ...

When the TH LED on the front panel is lit amber after a successful boot-up, it indicates that the processor die temperature is above 100°C.

6.2.4 Thermal Monitor 2 (TM2)

The Thermal Monitor 2 (TM2) Sensor controls the processor temperature and power consumption using the Intel® Speedstep® function, which is always available to TM2 when the processor silicon reaches its maximum operating temperature (100°C).

When TM2 is enabled and a high temperature situation exists, the processor will perform an Enhanced Intel® SpeedStep® Technology transition to a lower operating point and reports to a throttle event the BMC, which is reflected in the CPU0 status sensors. In this case, the processor reduces its operating frequency and processor core voltage. This combination of reduced frequency and core voltage results in a reduction of the processor power consumption. When the processor temperature is again within specification, TM2 returns the processor to the last requested SpeedStep® state.

The temperature at which TM2 activates the Intel® Speedstep® function is neither user-configurable nor software-visible.

TM2 does not require any additional hardware, software drivers, or interrupt handling routines. This function can be enabled and disabled in the BIOS.

Note ...

When the TH LED on the front panel is lit amber after a successful boot-up, it indicates that the processor die temperature is above 100°C.

6.2.5 TM1 and TM2 Operation

TM1 and TM2 are built-in functions of the CPU. They can be enabled or disabled via the BIOS. When the Thermal Monitor is enabled, TM2 has priority over TM1. If TM2 does not provide sufficient temperature reduction, TM1 will be activated in addition to TM2. If the Thermal Monitor is disabled, the CPU is operated out-of-specification.

6.2.6 Catastrophic Cooling Failure Sensor

The Catastrophic Cooling Failure Sensor protects the processor from catastrophic overheating. The Catastrophic Cooling Failure Sensor threshold is set well above the maximum operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 125°C. Once activated, the event remains latched until the CP6001 undergoes a power-on restart (all power off and then on again).

This function cannot be enabled or disabled in the BIOS. It is always enabled to ensure that the processor is protected in any event.

Note ...

When the TH LED on the front panel is blinking red/green after a successful boot-up, it indicates that the processor die temperature is above 125°C.

6.3 External Thermal Regulation

To ensure the best possible basis for operational stability and long-term reliability, the R1 version is equipped with a heat sink, and the R2 version is equipped with a heat sink and stiffeners. Coupled together with system chassis, which provide variable configurations for forced airflow, controlled active thermal energy dissipation is guaranteed. The physical size, shape, and construction of the heat sink and heat spreader ensures the lowest possible thermal resistance. In addition, they have been specifically designed to efficiently support forced airflow and convection cooling concepts as found in modern CompactPCI systems. The CP6001 must not be operated without the minimum required forced airflow.

Thermal Characteristic Graphs

The thermal characteristic graphs shown on the following sections illustrate the maximum ambient air temperature as a function of the volumetric airflow rate for the power consumption indicated. The diagrams are intended to serve as guidance for reconciling board and system with the required computing power considering the thermal aspect. One diagram per CPU version is provided. There are up to two curves representing upper level working points based on different levels of average CPU utilization. When operating below the corresponding curve, the CPU runs steadily without any intervention of thermal supervision. When operated above the corresponding curve, various thermal protection mechanisms may take effect resulting in temporarily reduced CPU performance or finally in an emergency stop in order to protect the CPU from thermal destruction. In real applications this means that the board can be operated temporarily at a higher ambient temperature or at a reduced flow rate and still provide some margin for temporarily requested peak performance before thermal protection will be activated.

An airflow of 2.0 m/s to 2.5 m/s is a typical value for a standard *Kontron* ASM rack (6U CompactPCI rack with a 1U cooling fan tray). For other racks or housings the available airflow will differ. The maximum ambient operating temperature must be recalculated and/or measured for such environments. For the calculation of the maximum ambient operating temperature, the processor and chipset junction temperature must never exceed the specified limit for the involved processor and chipset.

TDP curves

- 100% TDP curve
  This load complies with the maximum thermal design power (TDP) indicated in Chapter 5.2 Power Consumption, Table 5-7. 100% TDP can be achieved through the use of specific tools to heat up the CPU but 100% TDP is unlikely to be reached in real applications.
- 75% TDP curve
  This load represents a "typical" maximum power consumption reached under OS controlled applications. Typically, this load corresponds with 75% of the TDP (see Chapter 5.2 Power Consumption, Table 5-6).

How to read the diagram

Select a specific CPU and choose a specific working point indicated in TDP percentage. For a given flow rate there is a maximum airflow input temperature (= ambient temperature) provided. Below this operating point, thermal supervision will not be activated. Above this operating point, thermal supervision will become active protecting the CPU from thermal destruction. The minimum airflow rate provided must not be less than the value specified in the diagram.

Volumetric flow rate

The volumetric flow rate refers to an airflow through a fixed cross-sectional area (i.e. slot width x depth. The volumetric flow rate is specified in m^3/h (cubic-meter-per-hour) or cfm (cubic-feet-per-minute) respectively.

Conversion: 1 cfm = 1.7 m^3/h; 1 m^3/h = 0.59 cfm

Airflow

At a given cross-sectional area and a required flow rate, an average, homogeneous airflow speed can be calculated using the following formula:

Airflow = Volumetric flow rate / area.

The airflow is specified in m/s (meter-per-second) or in fps (feet-per-second) respectively.

Conversion: 1 fps = 0.3048 m/s; 1 m/s = 3.28 fps

The following figures illustrate the operational limits of the CP6001 taking into consideration power consumption vs. ambient air temperature vs. airflow rate. The measurements were made based on a 4HP slot and with both processor cores enabled.

6.3.1 Operational Limits for the R1 Version

Figure 6-2: Operational Limits for the R1 Version with Core™ Duo 1.2 GHz

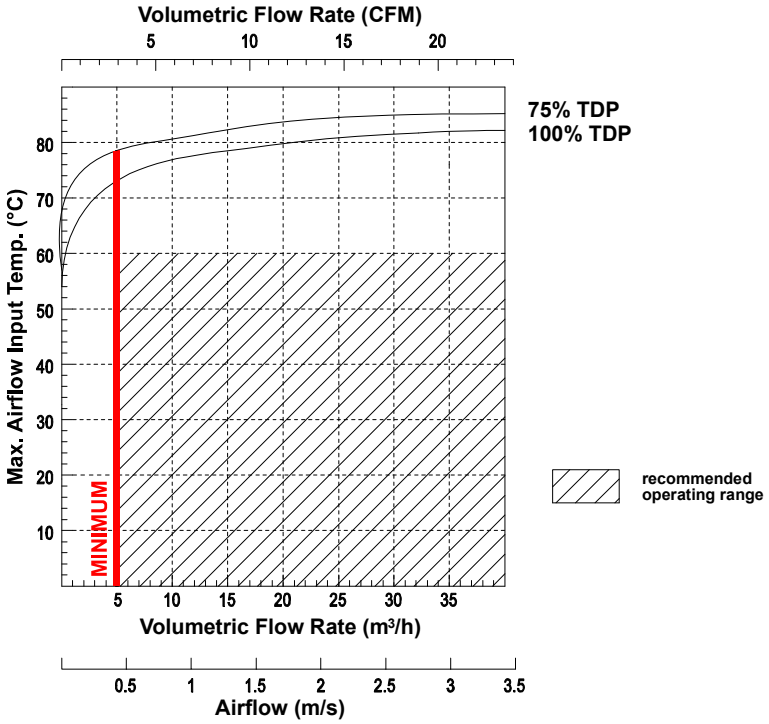
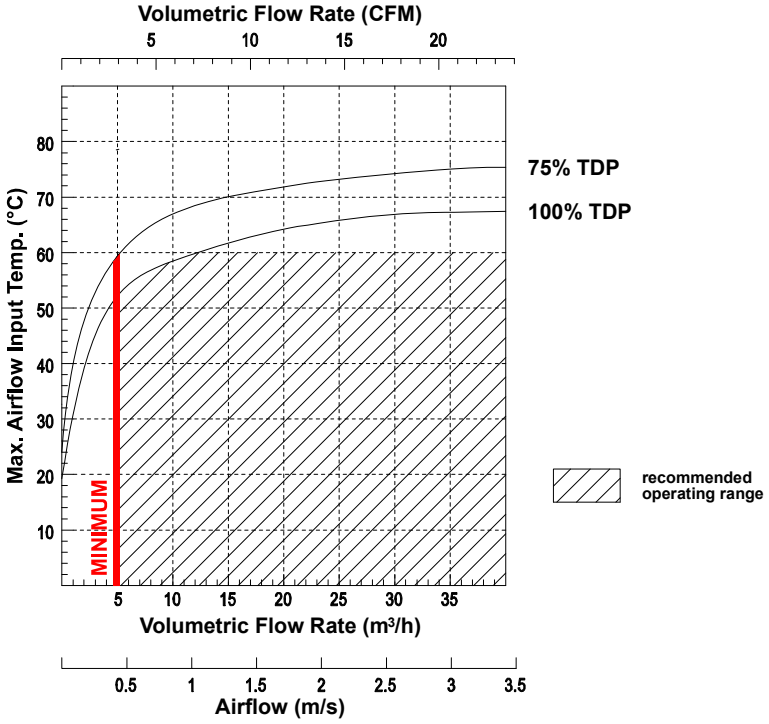


Figure 6-3: Operational Limits for the R1 Version with Core™2 Duo 1.5 GHz



6.3.2 Operational Limits for the R2 Version

Figure 6-4: Operational Limits for the R2 Version with Core™ Duo 1.2 GHz

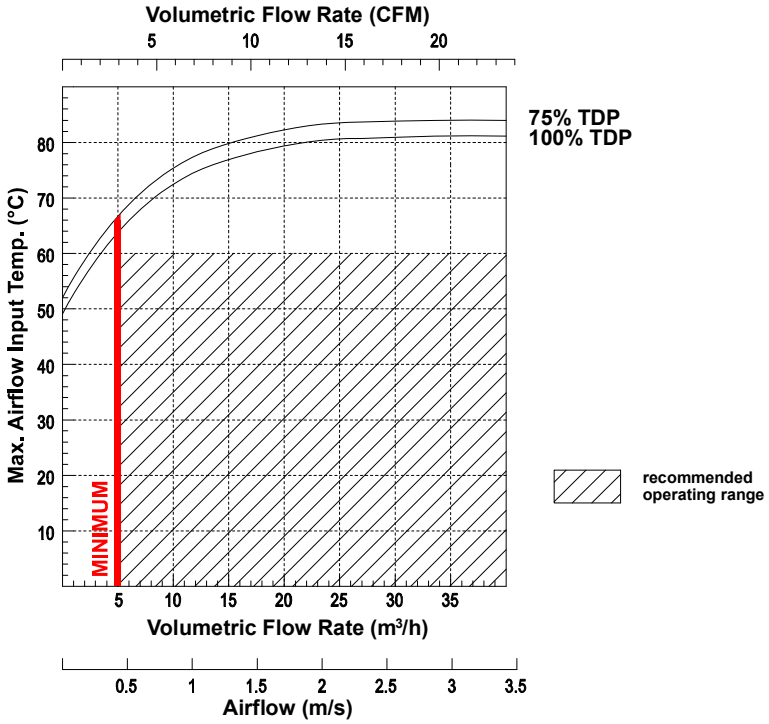
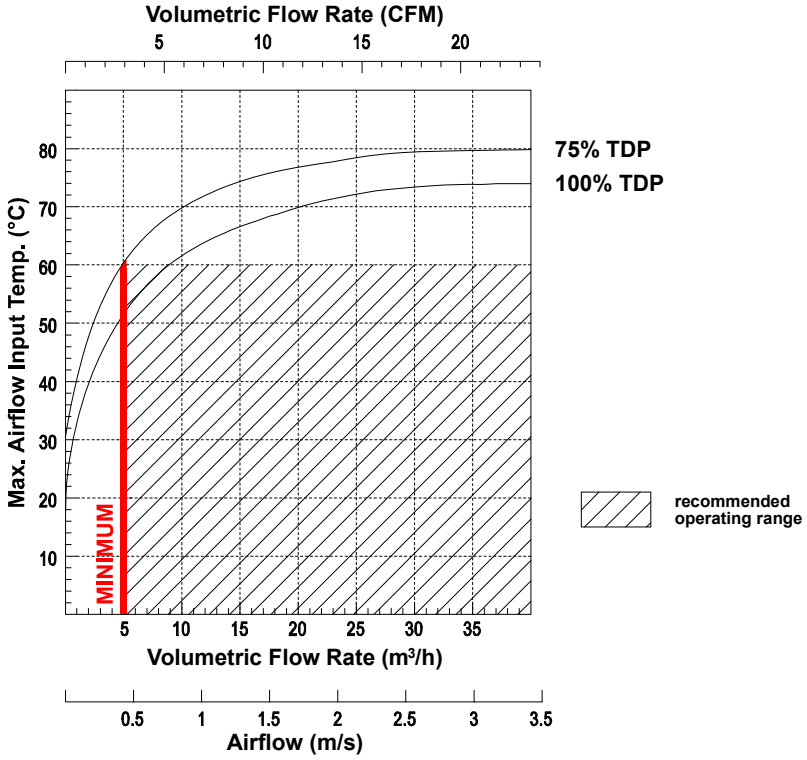


Figure 6-5: Operational Limits for the R2 Version with Core™2 Duo 1.5 GHz



6.3.3 Peripherals

When determining the thermal requirements for a given application, peripherals to be used with the CP6001 must also be considered. Devices such as hard disks, PMC modules, etc. which are directly attached to the board must also be capable of being operated at the temperatures foreseen for the application. It may very well be necessary to revise system requirements to comply with operational environment conditions. In most cases, this will lead to a reduction in the maximum allowable ambient operating temperature or even require active cooling of the operating environment.

Warning!

As Kontron assumes no responsibility for any damage to the CP6001 or other equipment resulting from overheating of the CPU or any other board components, it is highly recommended that system integrators as well as end users confirm that the operational environment of the CP6001 complies with the thermal considerations set forth in this document.

Appendix A

CP6001-MK2.5SATA

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A. CP6001-MK2.5SATA Assembly Kit

The optional CP6001-MK2.5SATA assembly kit includes one CP6001-EXT-SATA module and the necessary components required for mounting the module on the CP6001 R1 version.

A.1 CP6001-EXT-SATA Module Overview

The CP6001-EXT-SATA module has been designed to connect an onboard 2.5" Serial ATA hard disk drive to the CP6001 R1 version.

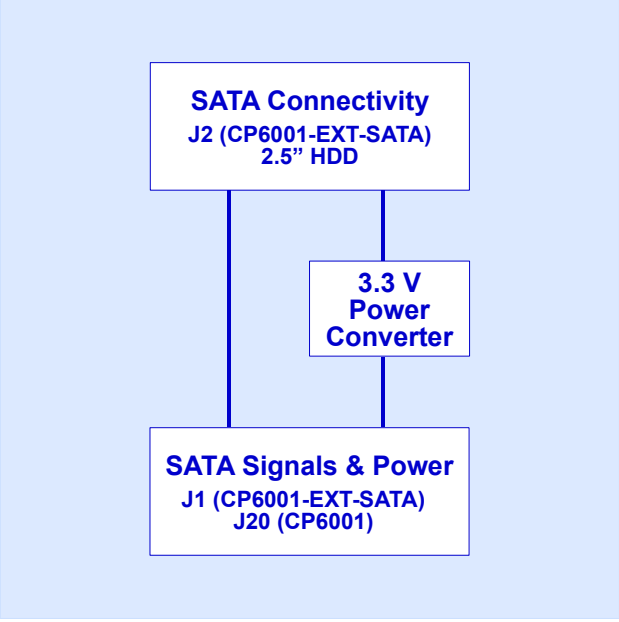
A.2 Technical Specifications

Table A-1: CP6001-EXT-SATA Main Specifications

CP6001-EXT-SATA		SPECIFICATIONS
Interfaces	Board-to-Board Connector	One 12-pin, male, board-to-board connector, J1
	Serial ATA Connector	One 22-pin Serial ATA connector, J2
General	Power Consumption	3.3 V or 5 V, depending on the hard disk Current 2.5” Serial ATA HDDs do not use 3.3 V.
	Temperature Range	Operating temp.: 0°C to +60°C Storage temp.: -55°C to +85°C
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	54 mm x 27.5 mm
	Board Weight	ca.6 grams (without hard disk)

A.3 CP6001-EXT-SATA Functional Block Diagram

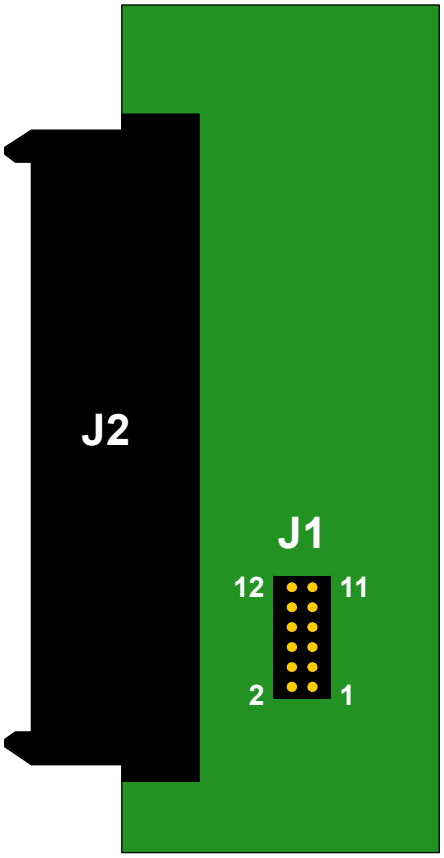
Figure A-1: CP6001-EXT-SATA Functional Block Diagram



A.4 CP6001-EXT-SATA Module Layout

The CP6001-EXT-SATA module includes one board-to-board connector, J1, and one SATA connector, J2.

Figure A-2: CP6001-EXT-SATA Module Layout



A.5 Module Interfaces

A.5.1 Board-to-Board Connectors J1

The board-to-board connector, J1, on the CP6001-EXT-SATA module is connected to the SATA extension connector, J20, on the CP6001.

Table A-2: Board-to-Board Connector J1 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	SATA_RX-	Differential Receive -	O
2	GND	Ground signal	--
3	SATA_RX+	Differential Receive +	O
4	GND	Ground signal	--
5	GND	Ground signal	--
6	5V	5V power	--
7	SATA_TX-	Differential Transmit -	I
8	GND	Ground signal	--
9	SATA_TX+	Differential Transmit +	I
10	GND	Ground signal	--
11	GND	Ground signal	--
12	5V	5V power	--

A.5.2 SATA Connector J2

The SATA connector, J2, on the CP6001-EXT-SATA module is connected to the 2.5” SATA HDD mounted on the CP6001. The SATA connector is divided into two segments, a signal segment and a power segment.

Figure A-3: SATA Connector J2

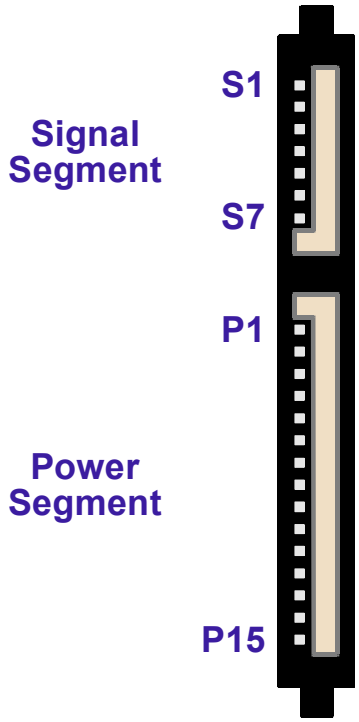


Table A-3: SATA Connector J2 Pinout

PIN	SIGNAL	FUNCTION	I/O
Signal Segment Key			
S1	GND	Ground signal	--
S2	SATA_TX+	Differential Transmit+	I
S3	SATA_TX-	Differential Transmit-	I
S4	GND	Ground signal	--
S5	SATA_RX-	Differential Receive-	O
S6	SATA_RX+	Differential Receive+	O
S7	GND	Ground signal	--
Signal Segment “L”			
Central Connector Polarizer			
Power Segment “L”			
P1	3.3V	3.3V power	--
P2	3.3V	3.3V power	--
P3	3.3V	3.3V power	--
P4	GND	Ground signal	--
P5	GND	Ground signal	--
P6	GND	Ground signal	--
P7	5V	5V power	--
P8	5V	5V power	--
P9	5V	5V power	--
P10	GND	Ground signal	--
P11	RES	Reserved	--
P12	GND	Ground signal	--
P13	12V (NC)	Not connected	--
P14	12V (NC)	Not connected	--
P15	12V (NC)	Not connected	--
Power Segment Key			

Appendix B

CP-RIO6-001 Module

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B. CP-RIO6-001 Rear I/O Module

B.1 Overview

The CP6001 provides optional rear I/O connectivity for peripherals, a feature which may be particularly useful in specialized CompactPCI systems. Some standard PC interfaces are implemented and assigned to the front panel and to the rear I/O connectors J3-J5 on the CP6001.

When the CP-RIO6-001 rear I/O module is used, some of the main board/front panel connectors' signals are routed to the module interface. Thus, the CP-RIO6-001 rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For the system rear I/O feature a special backplane is necessary. The CPU board with rear I/O is compatible with all standard CompactPCI passive backplanes with rear I/O support.

The CP-RIO6-001 rear I/O module provides the following interfaces.

- CompactPCI rear I/O
- Three USB 2.0 ports, two on the front panel and one onboard for USB NAND Flash
- Two Gigabit Ethernet ports with LED signals
- Two COM ports
- Up to two digital video ports
- Up to two SATA ports
- Two fan connectors with PWM control and sense inputs to monitor the fan speed

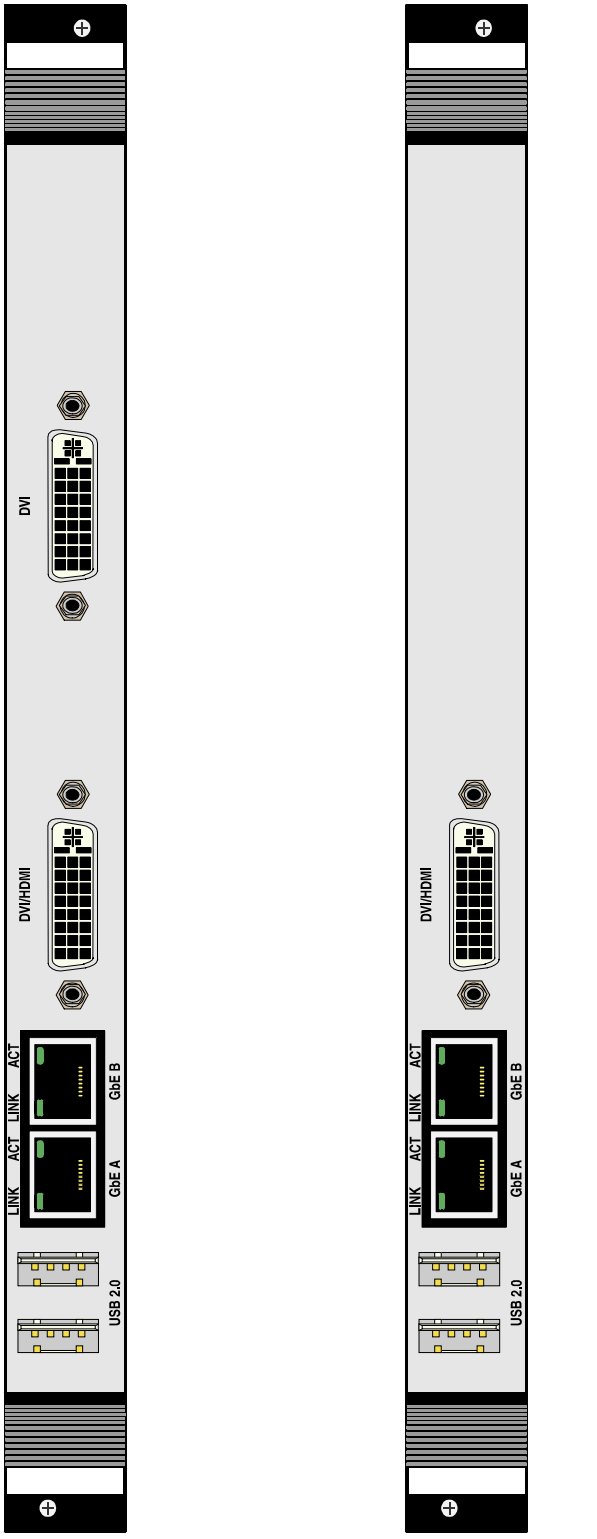
B.2 Technical Specifications

Table B-1: CP-RIO6-001 Main Specifications

CP-RIO6-001		SPECIFICATIONS
External Interfaces	USB	Two USB 2.0 interfaces on type A connectors
	DVI	Up to two DVI interfaces on DVI-I connectors: • One DVI/HDMI interface • One DVI interface (only on standard version)
	Ethernet	Two Gigabit Ethernet interfaces implemented as a dual RJ-45 connector
Internal Interfaces	SATA	Up to two SATA interfaces: • One SATA connector for connecting a SATA cable • One SATA connector for connecting a 2.5" HDD (optional)
	USB	One onboard connector for USB 2.0 NAND Flash module
	COM	Two onboard COM ports implemented as two 10-pin, 2.54 mm onboard connectors: • One serial port with RS-232 signaling • One serial port with RS-422 signaling
	Fan	Two fan connectors
	Compact PCI	Three CompactPCI connectors for connecting the rear I/O module to the backplane
General	Temperature Range	Operational: 0°C to +60°C Standard -40°C to +85°C E2 (optional) Storage: -55°C to +85°C Without any additional components ***Note ...*** When additional components are is installed, refer to their operational specifications as this will influence the operational and storage temperature of the CP-RIO6-001 module.
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	233.35 mm x 80 mm
	Board Weight	Standard version: 224 g (without USB NAND Flash module) Version with onb. HDD support: 218 g (without HDD and USB NAND Flash module)

B.3 Front Panels

Figure B-1: CP-RIO6-001 Front Panels



B.4 CP-RIO6-001 Rear I/O Module Layout

Figure B-2: CP-RIO6-001 Rear I/O Module Layout, Standard Version

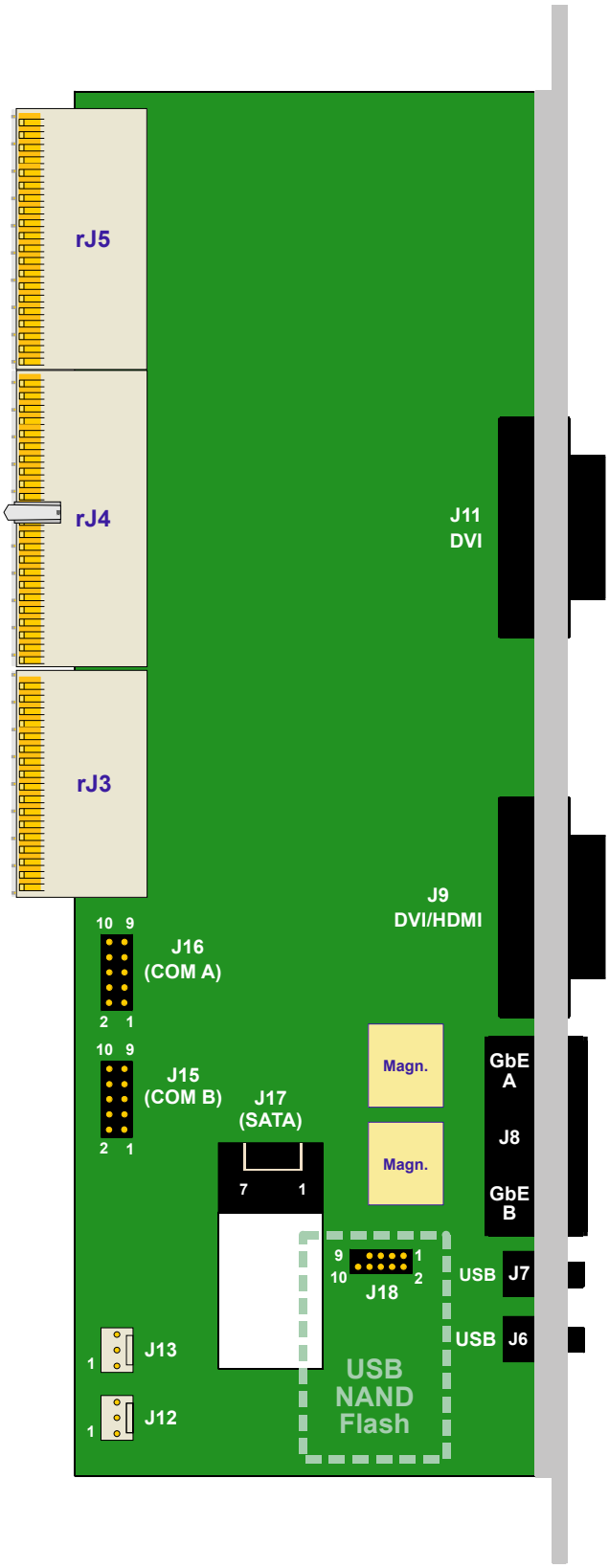
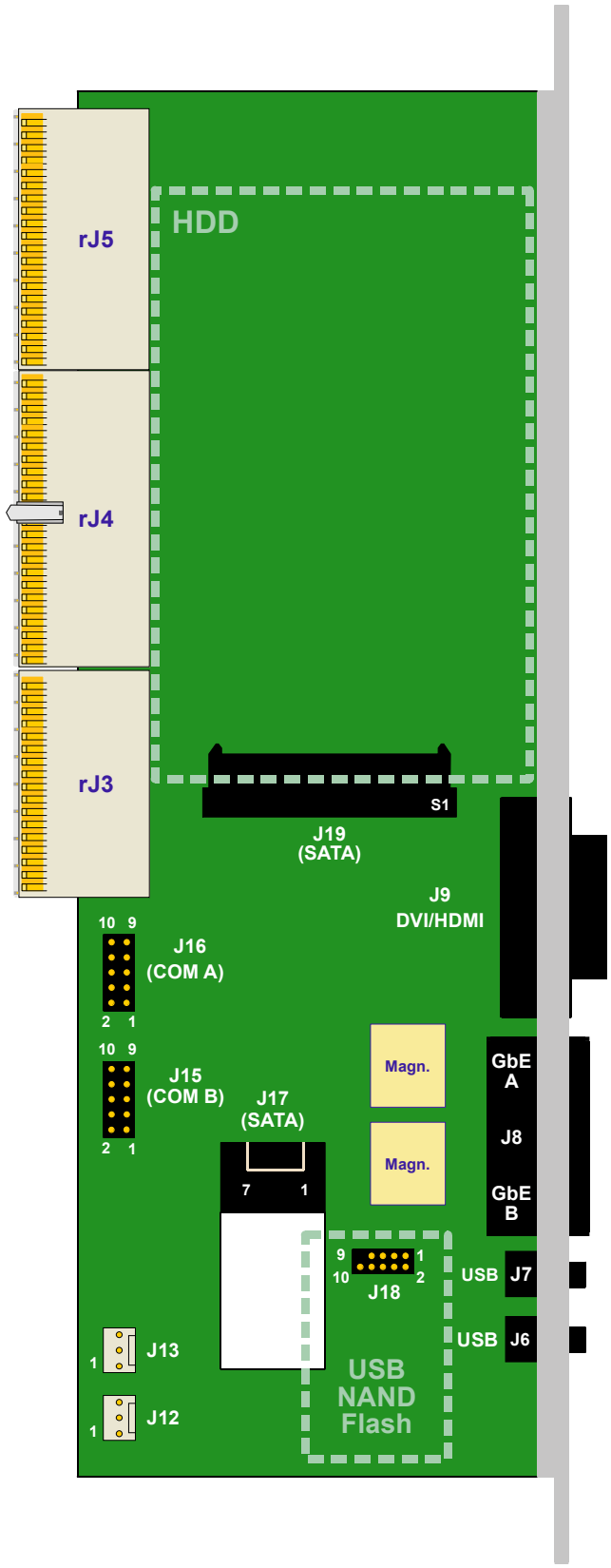


Figure B-3: CP-RIO6-001 Rear I/O Module Layout, Version with Onboard HDD Support



B.4.1 USB Interfaces

The CP-RIO6-001 rear I/O module supports three USB 2.0 ports, two on the front I/O and one onboard for USB NAND Flash module. All ports are high-speed, full-speed, and low-speed capable. High-speed USB 2.0 allows data transfers of up to 480 Mb/s - 40 times faster than a full-speed USB (USB 1.1).

One USB peripheral may be connected to each port. For connecting more USB devices to the CP6001 than there are available ports, an external USB hub is required.

Note ...

The USB host interfaces can be used with maximum 500 mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short-circuit protection is provided. All the signal lines are EMI-filtered.

Note ...

The rear I/O interface supports the USB 1.1 and USB 2.0 standards. For USB 2.0 it is strongly recommended to use a cable length not exceeding 3 meters.

B.4.1.1 Front Panel USB Connectors J6 and J7

On the front panel of the CP-RIO6-001 rear I/O module, there are two USB interfaces implemented on two 4-pin connectors with the following pinout:

Figure B-4: USB Con. J6 and J7

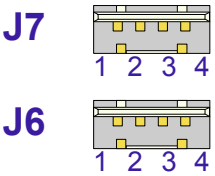


Table B-2: USB Con. J6 and J7 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	VCC	VCC	--
2	UV0-	Differential USB-	I/O
3	UV0+	Differential USB+	I/O
4	GND	GND	--

B.4.1.2 Onboard USB NAND Flash Connector J17

The CP-RIO6-001 rear I/O module has one onboard USB interface implemented on a 9-pin connector with the following pinout.

Figure B-5: USB NAND Flash Con. J17

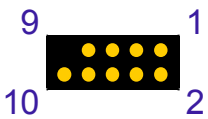


Table B-3: USB NAND Flash Con. J17 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	VCC	VCC	--
3	UV0-	Differential USB-	I/O
5	UV0+	Differential USB+	I/O
7	GND	GND	--
9	Key		
2, 4, 6, 8	NC	Not connected	--
10	Res.	Reserved	--

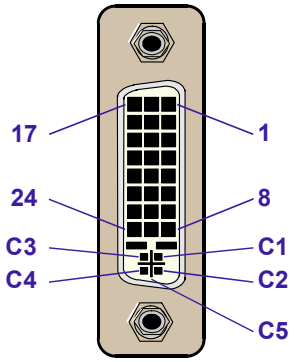
B.4.2 DVI Interfaces

The CP-RIO6-001 rear I/O module provides one DVI/HDMI interface. Additionally, one DVI interface is provided on the standard version to enable dual head support.

B.4.2.1 DVI/HDMI Connector J9

The DVI/HDMI connector J9 enables users to connect a monitor to the CP-RIO6-001 rear I/O module.

Figure B-6: DVI/HDMI Connector J9



The following table indicates the pinout of the DVI Connector J9.

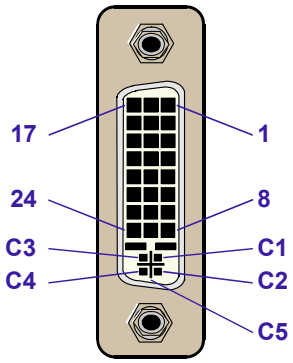
Table B-4: DVI Connector J9 Pinout

PIN	SIGNAL	DESCRIPTION	I/O	PIN	SIGNAL	DESCRIPTION	I/O
1	TMDS Data 2-	TMDS* Link -	O	2	TMDS Data 2+	TMDS* Link +	O
3	GND	Ground	--	4	NC	Not connected	--
5	NC	Not connected	--	6	DDC Clock	I^2C™ Clock	O
7	DDC Data	I^2C™ Data	I/O	8	NC	Not connected	--
9	TMDS Data 1-	TMDS Link -	O	10	TMDS Data 1+	TMDS Link +	O
11	GND	Ground	--	12	NC	Not connected	--
13	NC	Not connected	--	14	VCC	Power +5 V, 0.5A fused	--
15	GND	Ground	--	16	HPDETECT	Hot Plug Detect	I
17	TMDS Data 0-	TMDS Link -	O	18	TMDS Data 0+	TMDS Link +	O
19	GND	Ground	--	20	NC	Not connected	--
21	NC	Not connected	--	22	GND	Ground	--
23	TMDS Clock +	TMDS Link +	O	24	TMDS Clock -	TMDS Link -	O
C1	NC	Not connected	--	C2	NC	Not connected	--
C3	NC	Not connected	--	C4	NC	Not connected	--
C5	GND	Ground	--				

B.4.2.2 DVI Connector J11

The DVI connector J11 enables users to simultaneously connect a second monitor to the CP-RIO6-001 rear I/O module. This feature is referred to as dual head.

Figure B-7: DVI Connector J11



The following table indicates the pinout of the DVI Connector J11.

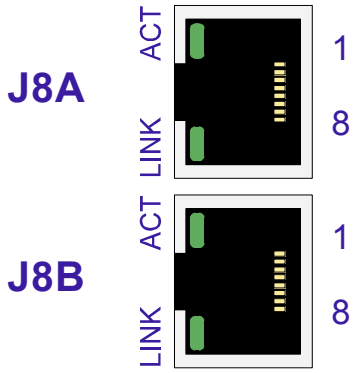
Table B-5: DVI Connector J11 Pinout

PIN	SIGNAL	DESCRIPTION	I/O	PIN	SIGNAL	DESCRIPTION	I/O
1	TMDS Data 2-	TMDS* Link -	O	2	TMDS Data 2+	TMDS* Link +	O
3	GND	Ground	--	4	NC	Not connected	--
5	NC	Not connected	--	6	DDC Clock	I^2C™ Clock	O
7	DDC Data	I^2C™ Data	I/O	8	NC	Not connected	--
9	TMDS Data 1-	TMDS Link -	O	10	TMDS Data 1+	TMDS Link +	O
11	GND	Ground	--	12	NC	Not connected	--
13	NC	Not connected	--	14	VCC	Power +5 V, 0.5A fused	--
15	GND	Ground	--	16	HPDETECT	Hot Plug Detect	I
17	TMDS Data 0-	TMDS Link -	O	18	TMDS Data 0+	TMDS Link +	O
19	GND	Ground	--	20	NC	Not connected	--
21	NC	Not connected	--	22	GND	Ground	--
23	TMDS Clock +	TMDS Link +	O	24	TMDS Clock -	TMDS Link -	O
C1	NC	Not connected	--	C2	NC	Not connected	--
C3	NC	Not connected	--	C4	NC	Not connected	--
C5	GND	Ground	--				

B.4.3 Gigabit Ethernet Interface

The Ethernet connectors are realized as RJ-45 connectors. The interface provides automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto MDI-X).

Figure B-8: Dual Gigabit Ethernet Connector J8A/B



RJ-45 Connector J8A/B Pinout

The J8A/B connector supplies the 10Base-T, 100Base-TX and 1000Base-T interfaces to the Ethernet controller.

Table B-6: Pinout of J8A/B Based on the Implementation

MDI / STANDARD ETHERNET CABLE						PIN	MDIX / CROSSED ETHERNET CABLE					
10BASE-T		100BASE-TX		1000BASE-T			10BASE-T		100BASE-TX		1000BASE-T	
I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL		I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
O	TX+	O	TX+	I/O	BI_DA+	1	I	RX+	I	RX+	I/O	BI_DB+
O	TX-	O	TX-	I/O	BI_DA-	2	I	RX-	I	RX-	I/O	BI_DB-
I	RX+	I	RX+	I/O	BI_DB+	3	O	TX+	O	TX+	I/O	BI_DA+
-	-	-	-	I/O	BI_DC+	4	-	-	-	-	I/O	BI_DD+
-	-	-	-	I/O	BI_DC-	5	-	-	-	-	I/O	BI_DD-
I	RX-	I	RX-	I/O	BI_DB-	6	O	TX-	O	TX-	I/O	BI_DA-
-	-	-	-	I/O	BI_DD+	7	-	-	-	-	I/O	BI_DC+
-	-	-	-	I/O	BI_DD-	8	-	-	-	-	I/O	BI_DC-

Note ...

The Ethernet transmission can operate effectively with structured cable that meets CAT5 cable or higher specifications.

Ethernet LED Status

ACT (green): This LED monitors network connection and activity. When this LED is lit, it means that a link has been established. The LED blinks when network packets are sent or received through the RJ-45 port. When this LED is not lit, there is no link established.

LINK (green): This LED lights up to indicate a successful 100Base-TX connection. When not lit and the ACT-LED is active, the connection is operating at 1000Base-T or 10Base-T.

B.4.4 Serial ATA Interfaces

The CP-RIO6-001 rear I/O module provides up to two Serial ATA (SATA) interfaces. Both interfaces are capable of supporting SATA I (1.5 Gbit/sec) and SATA II (3.0 Gbit/sec) signaling. One of the SATA interfaces is used for mounting an onboard 2.5" HDD. The other SATA interface is used for connecting standard SATA devices via a SATA cable.

B.4.4.1 SATA Connector J17

The SATA connector J17 is used to connect standard HDDs and other SATA devices to the CP-RIO6-001 rear I/O module via a SATA cable. The CP-RIO6-001 rear I/O module will not exceed the thickness of 4HP when a Serial ATA cable is used.

The following figure and table provide pinout information for the SATA connector J17.

Figure B-9: SATA Con. J17

Table B-7: SATA Connectors J17 Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	GND	Ground signal	--
2	SATA_TX+	Differential Transmit +	O
3	SATA_TX-	Differential Transmit -	O
4	GND	Ground signal	--
5	SATA_RX-	Differential Receive -	I
6	SATA_RX+	Differential Receive +	I
7	GND	Ground signal	--

B.4.4.2 SATA Connector J19 (optional)

The SATA connector J19 is used to connect a 2.5” SATA HDD to the CP-RIO6-001 rear I/O module and is divided into two segments, a signal segment and a power segment. This connector is available on the version with onboard HDD support only.

Figure B-10: SATA Connector J19

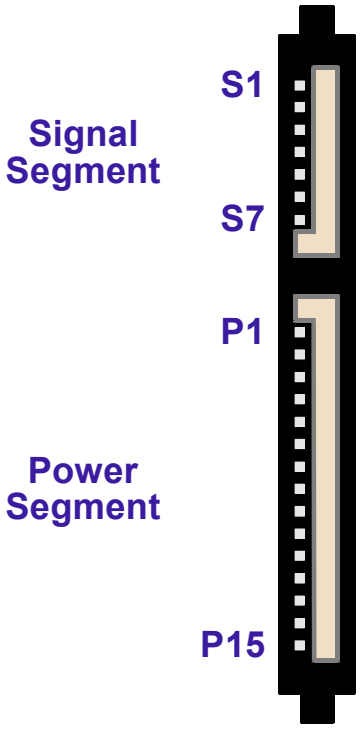


Table B-8: SATA Connector J19 Pinout

PIN	SIGNAL	FUNCTION	I/O
Signal Segment Key			
S1	GND	Ground signal	--
S2	SATA_TX+	Differential Transmit+	I
S3	SATA_TX-	Differential Transmit-	I
S4	GND	Ground signal	--
S5	SATA_RX-	Differential Receive-	O
S6	SATA_RX+	Differential Receive+	O
S7	GND	Ground signal	--
Signal Segment “L”			
Central Connector Polarizer			
Power Segment “L”			
P1	3.3V	3.3V power	--
P2	3.3V	3.3V power	--
P3	3.3V	3.3V power	--
P4	GND	Ground signal	--
P5	GND	Ground signal	--
P6	GND	Ground signal	--
P7	5V	5V power	--
P8	5V	5V power	--
P9	5V	5V power	--
P10	GND	Ground signal	--
P11	RES	Reserved	--
P12	GND	Ground signal	--
P13	12V	12 V power	--
P14	12V	12 V power	--
P15	12V	12 V power	--
Power Segment Key			

B.4.5 COM Interfaces

The CP-RIO6-001 rear I/O module provides two COM ports for connecting RS-232 (COMA) and RS-422 (COM2) devices.

The following figures and tables provide pinout information for the onboard COM connectors J15 (COM B) and J16 (COM A).

Figure B-11: Serial Port Con. J15 (COM B)

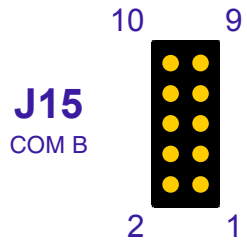


Table B-8: Serial Port Con. J15 (COM B) Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	RX+	Receive data +	I
2	RX-	Receive data -	I
3	NC	Not connected	--
4	NC	Not connected	--
5	TX+	Transmit data +	O
6	TX-	Transmit data -	O
7	NC	Not connected	--
8	NC	Not connected	--
9	NC	Not connected	--
10	NC	Not connected	--

Figure B-12: Serial Port Con. J16 (COM A)

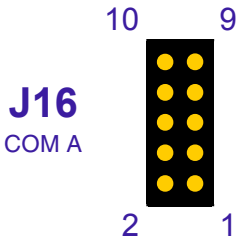


Table B-9: Serial Port Con. J16 (COM A) Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	DCD	Data carrier detect	I
2	DSR	Data send request	I
3	RXD	Receive data	I
4	RTS	Request to send	O
5	TXD	Transmit data	O
6	CTS	Clear to send	I
7	DTR	Data terminal ready	O
8	RI	Ring indicator	I
9	GND	Signal ground	--
10	NC	Not connected	--

B.4.6 FAN Connectors

The fan connectors J12 and J13 are used for connecting an external cooling fan to the CP-RIO6-001 rear I/O module.

Figure B-13: Fan Control Connectors J12 and J13

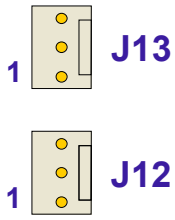


Table B-10: Fan Control Con. J12/J13 Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	GND	Ground signal	--
2	PWM	Fan Supply Voltage	O
3	SENSE	Fan Sense	I

B.4.7 Rear I/O interface on Compact PCI Connectors rJ2

The CP-RIO6-001 rear I/O module is equipped with three the CompactPCI rear I/O connectors, rJ3, rJ4 and rJ5.

Note ...

To support the rear I/O feature a corresponding backplane and CPU board are required.

Figure B-14: Rear I/O CompactPCI Connectors rJ3, rJ4 and rJ5

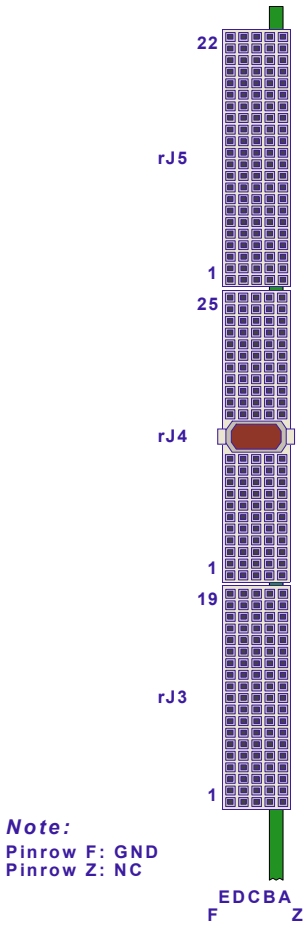


Table B-11: Rear I/O CompactPCI Rear I/O Connector rJ3 Pinout

PIN	Z	A	B	C	D	E	F
19	NC	RIO_VCC	RIO_VCC	RIO_3.3V	RIO_+12V	RIO_-12V	GND
18	NC	LPa_DA+	LPa_DA-	GND	LPa_DC+	LPa_DC-	GND
17	NC	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-	GND
16	NC	LPb_DA+	LPb_DA-	GND	LPb_DC+	LPb_DC-	GND
15	NC	LPb_DB+	LPb_DB-	GND	LPb_DD+	LPb_DD-	GND
14	NC	LPa:LINK	LPb:LINK	LPab:CT1	LPc:LINK	FAN:SENSE2	GND
13	NC	LPa:ACT	LPb:ACT	NC	NC	FAN:SENSE1	GND
12	NC	NC	NC	GND	NC	NC	GND
11	NC	NC	NC	GND	NC	NC	GND
10	NC	USB1:VCC	USB0:VCC	GND	RSV	USB2:VCC	GND
9	NC	USB1:D-	USB1:D+	GND	RSV	RSV	GND
8	NC	USB0:D-	USB0:D+	GND	USB2:D-	USB2:D+	GND
7	NC	RIO_3.3V	NC	ID3	ID4	SPEAKER	GND
6	NC	RSV	RSV	RSV	RSV	RSV	GND
5	NC	RSV	RSV	RSV	RSV	RSV	GND
4	NC	NC	NC	SP1:TX-	SP1:TX+	RSV	GND
3	NC	NC	NC	SP1:RX-	SP1:RX+	RSV	GND
2	NC	SP0:RI	SP0:DTR	SP0:CTS	SP0:TX	RSV	GND
1	NC	SP0:RTS	SP0:RX	SP0:DSR	SP0:DCD	ID1	GND

Warning!

The RIO_XXX signals are power supply **INPUTS** to supply the rear I/O module with power from the CP6001. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module.

Failure to comply with the above will result in damage to your board.

The following table describes the signals of the rJ3 connector.

Table B-12: Rear I/O CompactPCI Rear I/O Connector rJ3 Signals

SIGNAL	DESCRIPTION
SP0	COM1 Signaling (RS-232)
SP1	COM2 Signaling (RS-422)
USB0 to USB2	USB Port Signaling
SPEAKER	Standard PC Speaker
FAN	Fan Sensoring
LPa	Rear I/O LAN Port B
LPb	Rear I/O LAN Port A

Table B-13: Rear I/O CompactPCI Rear I/O Connector rJ4 Pinout

PIN	Z	A	B	C	D	E	F
25	NC	RSV	RSV	GND	RSV	RSV	GND
24	NC	RSV	RSV	GND	RSV	RSV	GND
23	NC	NC	RIO_VCC	GND	NC	RIO_3.3V	GND
22	NC	RSV	RSV	GND	RSV	RSV	GND
21	NC	RSV	RSV	GND	RSV	RSV	GND
20	NC	GND	GND	GND	GND	GND	GND
19	NC	RSV	RSV	GND	RSV	RSV	GND
18	NC	RSV	RSV	GND	RSV	RSV	GND
17	NC	GND	GND	GND	GND	GND	GND
16	NC	RSV	RSV	GND	RSV	RSV	GND
15	NC	RSV	RSV	GND	RSV	RSV	GND
12-14	Key Area						
11	NC	RSV	RSV	GND	RSV	RSV	GND
10	NC	RSV	RSV	GND	RSV	RSV	GND
9	NC	GND	GND	GND	GND	GND	GND
8	NC	RSV	RSV	GND	RSV	RSV	GND
7	NC	RSV	RSV	GND	RSV	RSV	GND
6	NC	GND	GND	GND	GND	GND	GND
5	NC	RSV	RSV	GND	RSV	RSV	GND
4	NC	RSV	RSV	GND	RSV	RSV	GND
3	NC	GND	GND	GND	GND	GND	GND
2	NC	RSV	RSV	GND	RSV	RSV	GND
1	NC	RSV	RSV	GND	RSV	RSV	GND

Warning!

The RIO_XXX signals are power supply **INPUTS** to supply the rear I/O module with power from the CP6001. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module.

Failure to comply with the above will result in damage to your board.

Table B-14: Rear I/O CompactPCI Rear I/O Connector rJ5 Pinout

PIN	Z	A	B	C	D	E	F
22	NC	RSV	PWM1:OUT	GND	PWM2:OUT	RSV	GND
21	NC	RSV	RSV	GND	RSV	RSV	GND
20	NC	RSV	RSV	GND	RSV	RSV	GND
19	NC	GND	GND	GND	RSV	RSV	GND
18	NC	DVI2:D0+	DVI2:D0-	GND	GND	GND	GND
17	NC	DVI2:D2+	DVI2:D2-	GND	DVI2:D1+	DVI2:D1-	GND
16	NC	RSV	DVI2:HPDET	GND	RSV	RSV	GND
15	NC	DVI2:CLK+	DVI2:CLK-	GND	DVI2:SDA	DVI2:SDC	GND
14	NC	GND	GND	GND	GND	GND	GND
13	NC	DVI1:D0+	DVI1:D0-	GND	DVI1:D1+	DVI1:D1-	GND
12	NC	DVI1:D2+	DVI1:D2-	GND	RSV	RSV	GND
11	NC	RSV	DVI1:HPDET	GND	DVI1:SDA	DVI1:SDC	GND
10	NC	DVI1:CLK+	DVI1:CLK-	GND	RSV	RSV	GND
9	NC	GND	GND	GND	GND	GND	GND
8	NC	HT3:TX+	HT3:TX-	GND	HT3:RX+	HT3:RX-	GND
7	NC	GND	GND	GND	GND	GND	GND
6	NC	RSV	RSV	GND	RSV	RSV	GND
5	NC	GND	GND	GND	GND	GND	GND
4	NC	HT1:TX+	HT1:TX-	GND	HT1:RX+	HT1:RX-	GND
3	NC	GND	GND	GND	GND	GND	GND
2	NC	RSV	RSV	GND	RSV	RSV	GND
1	NC	GND	GND	GND	GND	GND	GND

The following table describes the signals of the rJ5 connector.

Table B-15: Rear I/O CompactPCI Rear I/O Connector rJ5 Signals

SIGNAL	DESCRIPTION
HT1 and HT3	SATA Port 1 and Port 3 Signaling
DVI1	HDMI signaling
DVI2	DVI signaling
PWM	Pulse width modulation output for fan